Due in class Tuesday November 3.

To make life easier on the graders:
- Be sure your NAME and ECE MAILBOX NUMBER are prominently displayed on the upper right of what you hand in.
- When appropriate, indicate answers with a box or underline
- Work as neatly as possible

1. [ECE2019 refresher]

For the circuit shown in Figure 1a below,

a) find the $V_t$ and $R_t$ of the Thevenin equivalent for the circuit inside the dotted box.

b) Sketch the Thevenin equivalent circuit, being sure to indicate numerical values for $V_t$ and $R_t$.

c) As shown in Figure 1b, a load resistor $R_L = 2k\Omega$ is added to the circuit of Figure 1a. Determine the indicated load voltage $V_L$ and current $i_L$.

![Figure 1a.](image1.png)  ![Figure 1b.](image2.png)
2. [ECE2019 refresher]

In the figure below, use superposition to find voltage $v_1$.

![Figure with a 10kΩ resistor, a 6V source, and a 200μA current source]

3. [ECE2201 Microelectronics I refresher]

This problem concerns the circuit shown below. You have already performed an experiment on the "mystery component" in the box and determined that the output current $I_o$ depends only on $V_{IN}$. Your measured V-I data points are given in the table:

<table>
<thead>
<tr>
<th>$V_{IN}$ [V]</th>
<th>$I_o$ [$\mu$A]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>0</td>
</tr>
<tr>
<td>1.0</td>
<td>0</td>
</tr>
<tr>
<td>1.5</td>
<td>12</td>
</tr>
<tr>
<td>2.0</td>
<td>51</td>
</tr>
<tr>
<td>2.5</td>
<td>113</td>
</tr>
<tr>
<td>3.0</td>
<td>195</td>
</tr>
<tr>
<td>3.5</td>
<td>311</td>
</tr>
<tr>
<td>4.0</td>
<td>451</td>
</tr>
</tbody>
</table>

a) Plot $I_o$ as a function of $V_{IN}$ for the mystery component. Plot $V_{OUT}$ as a function of $V_{IN}$ for the circuit. Use a range of 0 to 4V for $V_{IN}$ in both cases.

b) Determine $V_{OUT}$ when $V_{IN} = 2.0V$.

c) Determine $V_{OUT}$ when $V_{IN} = 2.5V$.

d) Estimate $V_{OUT}$ when $V_{IN} = 2.25V$.

e) Estimate the small-signal transconductance $g_m = \Delta I_O/\Delta V_{IN}$ at an operating point of $V_{IN} = 2.25V$. Transconductance is the proportionality between a small change in the input voltage and the corresponding small change in the output current.

f) If $V_{IN}$ is a 100mV peak sine wave riding on a DC bias level of 2.25V $V_{IN} = 2.25V + (0.1V)\sin(2\pi ft)$ then estimate the DC bias level and the peak amplitude of the waveform at $V_{OUT}$.
4. [ECE2799 / Design principles refresher]

This problem concerns design of a voltage divider to provide an output voltage $v_L$ to a load. The application is for a laptop computer; the voltage source is an 18V power supply represented by $v_B$. The load current $i_L$ represents the current drawn by a microprocessor; the load voltage $v_L$ is nominally 3.3V and must remain between 3.0V and 3.6V for proper operation of the microprocessor chip.

The first approach is the voltage divider shown in the figure below. As we will see in this problem, the efficiency of the voltage divider is quite poor, resulting in excessive power consumption.

![Voltage Divider Diagram]

a) Design the voltage divider, choosing $R_1$ and $R_2$ to meet the following specifications:
   - $v_L = 3.6V$ for $i_L = 0$
   - $v_L = 3.0V$ for $i_L = 100mA$ (0.1A)

b) Given your design from (a), find the current $i_B$ drawn from the 18V source when $i_L=100mA$

c) Suppose the 18V source is a battery with capacity given as 2 Ampere-hours (A-hr). Find the battery life (in hours) under the load condition in (b). That is, given the value of current $i_B$ you calculated when $i_L=100mA$, how long until the 2 A-hr charge is gone?

d) Under the load condition in (b) with $i_L=100mA$, calculate
   i) The power absorbed by the load $p_L$
   ii) The power provided by the battery $p_B$
   iii) The efficiency ($p_L/p_B \times 100\%$)

Note the very low efficiency: this is why voltage regulators are used to develop power supply voltages in almost all applications.
5. [ECE3204 Microelectronics II refresher]

This problem concerns the design and specification of the system block shown in Figure 5. The system block has as its input a 100mV step. The output step should be inverted, and the amplitude should be 5V. The output DC error $V_e$ added by the system must be less than 100 mV. The 10%-to-90% rise time $t_r$ at the output must be less than 1µsec. The output should be a clean single-time-constant exponential; that is, there should be no slew-rate limiting. The output must drive a load resistance of 150Ω to ground. The input resistance of your design (looking into the $V_{IN}$ terminal) should be $\geq$ 1kΩ.

a) Draw an op-amp circuit that could perform the amplifying function required.

b) Determine the performance required of the op-amp for the following specification parameters:

- Gain-Bandwidth Product
- Slew Rate
- Maximum output current
- DC offset voltage (input referred)

NOTE: To solve this problem, you will need to recall some extremely important concepts from ECE3204, such as:

- Gain-Bandwidth product relationship
- Bandwidth - risetime relationship
- Time constant, 3-dB-frequency relationship
- Offset voltage model
- Amplifier input, output impedances
- Inverting, noninverting gain configurations
- Single time constant exponential
- Slew rate limiting
- Current limiting

If you are solid with these, you are in good shape for ECE4902. If not, visit a help session SOON to solidify your understanding! You've got to understand op-amps from the outside first before diving in to design and analyze them from the inside!
6. [Capacitance of reverse biased PN junction]

   Given a step PN junction with the following characteristics at T=300K:
   - Doping on P side: \( N_A = 2.0 \times 10^{22} \) acceptor / m\(^3\)
   - Doping on N side: \( N_D = 1.5 \times 10^{25} \) donor / m\(^3\)
   - Junction cross sectional area \( A_J = 200 \mu m^2 = 2.0 \times 10^{-10} m^2 \)

   a) Sketch a cross sectional view of the junction at zero bias, showing the depletion region and overall charge density (similar to the plots we did in class).

   b) Find the built-in voltage \( V_{bi} \) (SPICE parameter VJ) Note that, at T=300K, intrinsic carrier concentration is \( n_i = 1.0E+16 \) carrier / m\(^3\) and \( kT/q = 25.9 \) mV.

   c) Find the extent of the depletion region \( x_p \) into the P side and \( x_n \) into the N side at zero bias. Verify that the depletion region extends mostly into the lightly doped side.

   d) Find the small-signal junction capacitance per unit area for the zero bias condition (SPICE parameter CJ)

   e) For a step junction, the SPICE parameter for the junction capacitance exponent is \( MJ = 0.5 \). Using the small signal junction capacitance equation

\[
C_{j(\text{total})} = A_J \left( \frac{CJ}{1 + \left( \frac{V_R}{V_J} \right)^{MJ}} \right)
\]

find the total junction capacitance at zero bias and at a reverse bias of \( V_R = 5V \).
To answer the following questions on IC fabrication, you will need to read sections 17.1 through 17.7 of the Razavi textbook, as well as look at the Silicon Run video on reserve. We won’t get to this chapter in class until much later in the course, but I thought it would be a good idea to have you look at these problems while the Silicon Run video is still fresh in your mind.

7. [Processing steps]

Place the following processing steps in the correct order, give a brief description each, and the purpose of each step in construction of the MOSFET and/or connections between MOSFETs.

- Gate polysilicon deposition and patterning
- Field oxide deposition
- Gate oxide growth
- Contact and metal fabrication
- Channel-stop implant (also known as field implant)
- Source/drain junction implantation
- Well implantation

8. [Silicon Oxide]

a) List at least three roles that silicon dioxide SiO$_2$ plays in MOSFET integrated circuit operation and/or fabrication.

b) What is the meaning of the term "self-aligned"? What aspect of MOSFET fabrication does it refer to, and why is it important?

9. [Annealing]

a) What is annealing, and what is its intended purpose?

b) Give at least one unwanted consequence of annealing.

c) Why can't the IC be annealed after metal is deposited? (Hint: what is the melting point of the aluminum metal used for interconnection?)
10. [Capacitance of MOS gate]

Given a P-channel MOSFET with the following characteristics:

- \( W = 200 \ \mu m \)
- \( L = 5 \ \mu m \)
- Oxide thickness \( t_{ox} = 1.1 \times 10^{-8} \ \text{m} \)

a) Sketch a cross sectional view of the MOSFET in accumulation, depletion, and inversion (similar to the plots we did in class). Assume that \( V_{DS} = 0 \). In each case show clearly any electric field lines, the charges on which the field lines terminate, and the sign and kind of charge (e.g. mobile or fixed).

b) Determine the gate capacitance per unit area (in fF/\( \mu m^2 \)) in accumulation.

c) Determine the total capacitance from gate to channel in accumulation.
11. [IC Economics]

In the example given in class, we saw that (for the process and packaging given) reducing die size from 40mm$^2$ to 10mm$^2$ reduced the cost per die from around $60 to around $5. One question to ask is: how much better do things get if we keep pushing? Is there a limit or will the cost just keep going down?

a) Repeat the cost per good die calculation for a die size of 5mm$^2$, 2mm$^2$, 1mm$^2$, and 0.2mm$^2$. Be sure to revise the yield $Y_1$ based on die size using the chart below (the same one from lecture). Feel free to use a spreadsheet to automate the repeated calculations.

b) Plot the cost per die as a function of die size. You should see the cost per die approaching a limit. What determines the limit?
12. [Resistor design]

It is required to make an op-amp circuit with voltage gain = 2 using the noninverting circuit shown below. This problem concerns design of the resistor used for $R_1$ and $R_2$.

a) You are considering making the resistor out of one of the following layers:
   - Bottom metal layer (M1)
   - Polysilicon (POLY)
   - P-channel drain diffusion (P+)
   - N-well (N_W).

   How many squares are required in each case for a 10kΩ resistor? Use the process parameters handed out in class; also available at ece.wpi.edu/~mcneill/handouts/16umparameters.pdf

   Ignore the effects of contact resistance.

b) What length $L$ is required if a width of $W = 8 \, \mu m$ is used?

c) Compare the total area required for both resistors in each of the different layer options.

d) Find the parasitic capacitance from the resistor material to substrate in each case.

e) Given your results from (c) and (d), which layer is the best choice for a 10kΩ resistor in IC design, and why?
To avoid the DC power dissipation associated with resistors, most analog IC designs use capacitive voltage dividers in the op-amp feedback. An example is the gain-of-2 circuit shown below:

a) Show that the gain of the circuit is \( \frac{V_{OUT}}{V_{IN}} = 1 + \frac{C_1}{C_2} \)

b) You are considering whether to make the capacitor plates from poly-poly2 (POLY-POLY2) or metal1-metal2 (M1-M2). From the 1.6\( \mu \)m process parameters, what is the available capacitance per unit area in F/\( \mu \)m\(^2\) for each option? Estimate the area in \( \mu \)m\(^2\) required for a value of 1pF for each option. Which choice is better, and why?

c) You wisely decide that each capacitor is to be made from poly-poly2. For simplicity, the plates of the capacitor will be square (W=L) as shown. Determine the dimension required to realize the 1pF value indicated.

d) Now suppose that each dimension of each capacitor is subject to independent random variation of ±0.1\( \mu \)m. For example, a W of 10\( \mu \)m could be anywhere from 10.1\( \mu \)m to 9.9\( \mu \)m. For the op-amp circuit, what are the maximum and minimum possible gains for the "worst case" combinations of \( W_1, L_1, W_2, L_2 \)?

e) For a gain accuracy of 0.1\% (that is, gain between 1.998 and 2.002) even in the presence of random variation of ±0.1\( \mu \)m in capacitor dimensions, what W and L are required?

Thus the analog IC designer’s principle that to gain the benefit of improved matching, the price you usually pay is spending more area.