**ECE4902 B2015**

**HW Set 2**

Due in class Tuesday November 10. Note the more-compassionate-than-Set-1 number of problems - only seven - since

a) you should be starting to spend time on labs, and

b) you have Quiz 1 this Friday

To make life easier on the grader:

- Be sure your NAME and ECE MAILBOX NUMBER are prominently displayed on the upper right of what you hand in.
- When appropriate, indicate answers with a box or underline
- Work as neatly as possible

You may assume $T = 300K$ unless otherwise indicated.

1) [Mobility]

The table below provides measured data relating carrier velocity $v$ as a function of applied electric field $\mathcal{E}$ for mobile electrons in the channel of an n-channel MOSFET.

<table>
<thead>
<tr>
<th>$\mathcal{E}$ [V/cm]</th>
<th>$v$ [cm/sec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.00E+01</td>
<td>3.62E+04</td>
</tr>
<tr>
<td>1.00E+02</td>
<td>1.11E+05</td>
</tr>
<tr>
<td>3.00E+02</td>
<td>3.46E+05</td>
</tr>
<tr>
<td>1.00E+03</td>
<td>7.86E+05</td>
</tr>
<tr>
<td>3.00E+03</td>
<td>2.10E+06</td>
</tr>
<tr>
<td>1.00E+04</td>
<td>4.37E+06</td>
</tr>
<tr>
<td>3.00E+04</td>
<td>5.46E+06</td>
</tr>
<tr>
<td>1.00E+05</td>
<td>5.78E+06</td>
</tr>
</tbody>
</table>

a) Plot the data. Do two plots: one on linear axes, and one on log-log axes.

b) Determine the electron mobility $\mu_n$ for “small” field $\mathcal{E}$.

c) Using the mobility concept, we were able to relate MOSFET drain current ($I_D$) and drain-source voltage ($V_{DS}$) with a resistive $r_{DS(on)}$ model. However, as can be seen from your plots, for sufficiently large fields, the mobility concept’s proportional relationship $v = \mu \mathcal{E}$ doesn’t work anymore. When the field is “too large”, would you expect the measured current for an actual MOSFET to be greater than or less than predicted by the $r_{DS(on)}$ model? Don’t just say “more” or “less” – THINK about what the carriers are doing in the MOSFET channel and explain your answer in your own words.
2) [MOSFET operating region practice]

For each MOSFET below, determine the MOSFET operating region (active, triode, cutoff). Assume NMOS $V_{TH} = +1V$ and PMOS $V_{TH} = -1V$.

a)

\[ V_G = +3V \]
\[ V_D = +5V \]

b)

\[ V_G = +2V \]
\[ V_D = +2V \]

c)

\[ V_G = +0V \]
\[ V_D = +5V \]

d)

\[ V_G = +3V \]
\[ V_D = +1V \]

e)

\[ V_S = +5V \]
\[ V_G = +2V \]
\[ V_D = +1V \]

f)

\[ V_S = +5V \]
\[ V_G = +2V \]
\[ V_D = +4V \]

g)

\[ V_S = +5V \]
\[ V_G = +5V \]
\[ V_D = +1V \]

h)

\[ V_S = +5V \]
\[ V_G = +2V \]
3) [More MOSFET operating region practice]

For each MOSFET below, determine
a) the MOSFET operating region (active, triode, cutoff), and
b) the drain voltage $V_D$ and the DC drain current $I_D$.
Assume NMOS $V_{TH} = +1V$ and PMOS $V_{TH} = -1V$.

For both NMOS and PMOS, assume $\mu C_{ox} \frac{W}{L} = 2.0E - 4 \frac{A}{V^2}$.

a) $V_{DD} = +5V$

b) $V_{DD} = +5V$

c) $V_{DD} = +5V$

d) $V_{DD} = +5V$

e) $V_{DD} = +5V$

f) $V_{DD} = +5V$

g) $V_{DD} = +5V$

h) $V_{DD} = +5V$
4) [“Even digital is analog”]

We’ve looked at the common source circuit configuration as an inverting amplifier, using the MOSFET in the active region. However, the same circuit can be used as an inverting logic gate, using the MOSFET in the cutoff region (output high) and triode region (output low) to encode the two logic states. This problem is concerned with the large signal and small signal design of a logic gate.

The circuit shown in Fig. 3-1 is to be used as a logic inverter. Before CMOS processes (which provided both N-channel and P-channel MOSFETs on the same chip) were practical, the NMOS logic family implemented the logic inversion function with this circuit. The MOSFET is the N-channel MOSFET of the CD4007 array; use parameters $V_{tn} = 1.4V$, $\mu_n C_{ox} = 3.0E-5 A/V^2$, and $W/L = 350\mu m/10\mu m$.

a) Large signal: Choose $R$ so that an input of 2.5V corresponds to an output of 2.5V. This will ensure symmetric switching in a logic family with 0 and 5V logic levels).

b) Small signal: Determine the gain from $v_{in}$ to $v_{out}$ at an operating point of $V_{IN} = +2.5V$. Although it might seem irrelevant to worry about an “analog” concept like gain in a digital system, it is actually very important that the gain magnitude be greater than unity: if the gain is less than one, logic swings become smaller and smaller as a logic signal propagates through a sequence of gates, until the logic swing is too small to switch a gate at all.
5) [Alternative method of MOSFET parameter extraction and modeling]

In lab, we used the triode region measurements of $R_m$ to determine the threshold voltage $V_{th}$ and mobility $\mu_n$. We can also extract these parameters from measurements made in the active region. The following measurements are taken on the MOSFET circuit shown below. (For the purposes of this problem, you may ignore channel length modulation).

\[ \text{MOSFET Circuit} \]

\[ \begin{align*}
V_{GS} & \quad 1.15 \text{ V} \quad 63 \text{ $\mu$A} \\
V_{GS} & \quad 1.30 \text{ V} \quad 103 \text{ $\mu$A} \\
V_{GS} & \quad 1.40 \text{ V} \quad 152 \text{ $\mu$A} \\
V_{GS} & \quad 1.50 \text{ V} \quad 215 \text{ $\mu$A} \\
V_{GS} & \quad 1.65 \text{ V} \quad 313 \text{ $\mu$A}
\end{align*} \]

a) Plot $I_D$ as a function of gate-source voltage $V_{GS}$ on linear axes.

b) Plot the square root of $I_D$ as a function of $V_{GS}$. Determine the slope and x-intercept of a "best-fit" line through these data points. The best fit line can be determined graphically from a plot of the points, or numerically using a technique such as least squares fitting. Even if you use a purely numerical technique, it's an excellent idea to look at the plot and make sure that the data points fall on a line! There may be deviations from the model, at low currents (subthreshold conduction) and/or high currents (mobility reduction).

c) Show that, if the MOSFET follows the square law, the plot of $\sqrt{I_D}$ provides $V_{TH}$ directly, as the intercept with the $I_D=0$ axis. Also show that the slope of the line is

\[ \sqrt{\frac{\mu C_{ox}}{2}} \frac{W}{L} \]

and therefore knowing the $W/L$ ratio for M1 allows you to determine $\mu_n C_{ox}$.

d) Estimate the parameters $V_{TH}$ and $\mu_n C_{ox}$ for this MOSFET.

e) It is desired to use this MOSFET in a circuit operating at a DC drain current of $I_D=175 \mu$A. Determine the gate-source operating voltage $V_{GS}$ required to realize this operating point, and determine the resulting small-signal transconductance $g_m$. 
6) [Analog switch design]

The figure below shows part of a boost converter used in a power application. The inductor current $i_L$ can be as high as 2.0A. When the MOSFET is “on” ($V_{GS} = +5V$) it is required for efficiency reasons that the voltage drop across the MOSFET $V_{DS}$ be no greater than 0.15V.

Process parameters (from the AMI 1.6µm process available through MOSIS):

$$V_{TH} = 0.57 [V] \quad \mu_nC_{ox} = 7.14E-5 [A/V^2]$$

a) Determine the required $R_{on}$

b) Assuming a minimum length of 1.6µm, find the required $W$ to realize your $R_{on}$ from (a) given a +5V gate drive. Note the huge W/L ratio needed!
7) [Capacitance cost]

From a look through the DigiKey catalog, you can see that a 0.1µF ceramic capacitor costs anywhere from 2¢ to 40¢ ($0.02 to $0.40), depending on voltage rating, dielectric material, etc. Let's pick a value in the middle and say that it's $0.10, which means the cost of capacitance is approximately $1 for 1µF of capacitance, or $1/µF.

What is the cost of capacitance for a poly-poly capacitor? Use a capacitance per unit area of 0.6fF/µm², and a wafer cost of $4000 for a 20cm diameter wafer. To simplify the analysis, assume you made the entire wafer into a capacitance, and ignore yield loss and packaging cost.

Note from this high cost the economic incentive to avoid circuit techniques that require high capacitance values on-chip.