1) [Current mirror design]

A simple MOSFET current mirror circuit in the AMI 1.6µm process is shown below, with a plot of each device's drain current shown also. This problem is concerned with some aspects of the performance of this circuit, and how that performance could be improved.
First, the current source performance specs of the existing design:

a) From the plot of simulated data, determine the small-signal output resistance $R_{out}$.

b) What is the approximate lower limit of the output voltage compliance range (the minimum voltage at the drain of MOSFET N0 that will still allow N0 to be in the saturation region)?

Now, infer the MOSFET characteristics so we can change the design to improve performance:

c) What is the value of the channel length modulation parameter $\lambda_n$ for this MOSFET?

d) Given this channel length modulation parameter $\lambda_n$, what is the $\mu$m$/V$ scale factor for the 1.6$\mu$m AMI process? (See problem 6, part (a), of the previous problem set)
2) [Current mirror design]

In class, and in the design problems we’ve looked at, the value of L was just given. However, what is often done in practice is to design for L using the relationship between L and \( \lambda \). The requirements for a current source are usually in terms of:
- current \( I_D \),
- output resistance \( R_{out} \),
- compliance range (minimum output voltage before current source “crashes”)

For a simple mirror, design proceeds as follows:
- The output resistance \( R_{out} \) is just the MOSFET output resistance \( r_o \), which gives the necessary \( \lambda \) when \( I_D \) is known.
- From the required \( \lambda \), L is determined using the relationship between L and \( \lambda \).
- The compliance range determines the allowable gate overdrive \( (V_{GS} - V_{TH}) \), since that sets the "triode crash" boundary.
- Given the required \( (V_{GS} - V_{TH}) \) and \( I_D \), the ratio \( W/L \) is determined. Since L is already determined, W can be calculated.

It is required to increase the output resistance of the current source from the previous problem to 5M\( \Omega \), while keeping the value of the current and the compliance range unchanged.

a) What is the value of the channel length modulation parameter \( \lambda_n \) required to achieve the 5M\( \Omega \) output resistance of the current source?

b) Given that \( \lambda_n \) is inversely proportional to length L, what is the new length of the MOSFET necessary to achieve the required value of \( \lambda_n \)?

c) What is the new value of the channel width W required to keep the value of the current and the compliance range unchanged, given the new value of L from part (b)?

Note the greatly increased area of the new design! We will return to this design when we consider cascode current mirrors.
Use the following parameters for minimum length (L=1.6µm) devices for the MOSFETs in problems (3-7). You may assume T = 300K unless otherwise indicated.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N-channel</th>
<th>P-channel</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_t$</td>
<td>+0.57</td>
<td>-0.93</td>
<td>V</td>
</tr>
<tr>
<td>$\mu C_{ox}$</td>
<td>7.14E-5</td>
<td>2.40E-5</td>
<td>A/V^2</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.081</td>
<td>0.24</td>
<td>V^{-1}</td>
</tr>
</tbody>
</table>

3) [Analysis of common source amplifier with resistive load]

![Circuit Diagram]

a) Determine the value of $V_{BIAS}$ that will give an output operating point of $V_{OUT} = +3.0V$. Do not ignore channel length modulation!

b) Draw the small-signal model for the circuit.

c) Determine the small-signal transfer function $v_{out}/v_{s}$.

d) Determine low frequency gain and the bandwidth (3-dB frequency) and the unity-gain frequency $f_T$.

e) Carefully draw the magnitude and phase Bode plot for the transfer function.

f) Sketch the total output voltage $v_{OUT}$ vs time when $v_{in} = (+0.1V)\sin(2\pi[1kHz]t)$
4) [Design bias for common source amplifier with active load]

![Circuit Diagram](image)

The circuit in Fig. 4-3 is a common source amplifier with active load. Your task is to complete the design by determining:
- the input DC bias voltage $V_{IN}$
- the current mirror bias resistor $R_B$
- the DC drain current $I_D$
- width $W_1$ of the common source N-channel MOSFET M1
- width $W_2$ of the current mirror P-channel MOSFETs M2 and M3

to meet the following performance criteria:
- output DC bias of +2.5V
- output linear range of at least +0.5V to +4.5V (that is, $V_{OUT}$ can swing to within 0.5V of either rail without any MOSFET crashing in to triode
- Gain-bandwidth product (or, equivalently, unity-gain frequency) $f_T = 1$MHz

a) Specify $V_{IN}$, $R_B$, $I_D$, $W_1$, and $W_2$ necessary. Note that you cannot ignore channel length modulation! And, since the L of 4$\mu$m is different than the L of 1.6$\mu$m for which the $\lambda$ parameters are given in the table at the beginning of this problem set, you will need to scale the values of $\lambda$ you use in this problem accordingly.

b) Sketch the small signal model for your design.

c) Sketch the magnitude and phase Bode plot for the small signal gain $V_{OUT}/V_{IN}$ predicted by your small signal model.

d) Sketch the total output voltage $V_{OUT}$ vs time when $v_{in} = (+0.001V)\sin(2\pi[1kHz]t)$
When a MOSFET current mirror is used to realize the current source that biases the differential pair, we find that the common mode gain is nonzero – that is, the common mode rejection is not perfect. For the differential amplifier shown below, the nonideality of the MOSFET current source is represented by a $1\,\text{M}\Omega$ resistor in parallel with the $50$ $\mu\text{A}$ current source.

![Diagram of differential amplifier](image)

5) [Differential amplifier analysis; common mode gain; half circuit practice]

a) Draw the half-circuit representations for the common mode and differential mode circuits.

b) Determine the common mode and differential mode gains.

c) Sketch the total output waveforms $V_{O1}$ and $V_{O2}$ for a purely differential input of a $10$ mV peak sine wave.

d) Sketch the total output waveforms $V_{O1}$ and $V_{O2}$ for a common mode input of a $1$ V peak sine wave.
You are required to choose \( R_D \) and MOSFET width \( W \) for the circuit in Figure 5-3. You are given DC bias current \( I_D = 50\mu A \). Requirements:

- Total differential output voltage swing = \( \pm 4V \)
- Low-frequency differential voltage gain magnitude \(|a| = 15\)

a) Determine the value of \( R_D \) and \( W \)

b) Sketch the total outputs \( V_{o1} \) and \( V_{o2} \) and the differential output \( v_{od} = V_{o1} - V_{o2} \) for \( V_+ = (+0.1V)\sin(2\pi[1kHz]t) \) and \( V_- = (-0.1V)\sin(2\pi[1kHz]t) \)

c) Sketch the total outputs \( V_{o1} \) and \( V_{o2} \) and the differential output \( v_{od} = V_{o1} - V_{o2} \) for \( V_+ = -2V + (+0.1V)\sin(2\pi[1kHz]t) \) and \( V_- = -2V + (-0.1V)\sin(2\pi[1kHz]t) \)

d) Sketch the total outputs \( V_{o1} \) and \( V_{o2} \) and the differential output \( v_{od} = V_{o1} - V_{o2} \) for \( V_+ = (+1V)\sin(2\pi[1kHz]t) \) and \( V_- = (-1V)\sin(2\pi[1kHz]t) \)

e) Sketch the total outputs \( V_{o1} \) and \( V_{o2} \) and the differential output \( v_{od} = V_{o1} - V_{o2} \) for \( V_+ = +2V + (+1V)\sin(2\pi[1kHz]t) \) and \( V_- = +2V + (-1V)\sin(2\pi[1kHz]t) \)
7) [Active load]

In the circuit of Figure 5-3, replace the resistive load with a PMOS current mirror active load.

a) Using the minimum channel length, size the PMOS devices so the output DC operating point with zero differential input is +3.8V.

b) What is the expected small signal gain to the single-ended output from the differential input?

c) The output is loaded with a 100pF capacitive load to ground. What is the expected bandwidth $f_{-3db}$ of the small signal gain magnitude at the single-ended output?

d) What is the expected signal swing before clipping at the output? (Assume input common mode voltage of zero). Which devices crash into triode at each clipping limit?