Due in class Tuesday December 8.

You may assume $T = 300K$ unless otherwise indicated. Use the following MOSFET parameters for minimum length ($L=1.6\mu m$) devices in the AMI process:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N-channel</th>
<th>P-channel</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_t$</td>
<td>+0.57</td>
<td>-0.93</td>
<td>V</td>
</tr>
<tr>
<td>$\mu C_{ox}$</td>
<td>7.14E-5</td>
<td>2.40E-5</td>
<td>$A/V^2$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.081</td>
<td>0.24</td>
<td>$V^{-1}$</td>
</tr>
</tbody>
</table>

1) [Comparing design approaches]

Frequently in single supply designs, it is necessary to develop a reference voltage $V_{MID}$ halfway between ground and the positive $VDD$ supply voltage rail. To save power, it is usually desired to minimize the amount of current drawn by the network that develops $V_{MID}$. The figure below shows three possible approaches to this problem; to make the comparison reasonable, a goal of $10\mu A$ current draw is set for each approach.

In the first approach, $V_{MID1}$ is developed from a voltage divider of equal value resistors with a total resistance of $R_{TOTAL} = 5V/10\mu A = 500k\Omega$.

In the second approach, $V_{MID2}$ is at the midpoint of two diode-connected MOSFETs, $N0$ and $P0$. By choosing the lengths $LN$ and $LP$ appropriately, $V_{MID2}$ can be set to 2.5V with a drain current of $10\mu A$ in each device.

In the third approach, two identical PMOS devices $P1$ and $P2$ are used. Note that $P2$ has the body tied to the source terminal to eliminate the body effect.
When MOSFETs are used in low current applications with large $V_{GS}$, usually it is necessary to have $L > W$. In this case we choose $W=4\mu m$ and determine the lengths $L_N$ and $L_P$ necessary to realize the design goals. Note that since the $L > L_{min}=1.6\mu m$, the $\lambda$ parameters in the table will need to be adjusted.

a) Determine the lengths of the 250kΩ resistors, assuming a width of $W_R = 4\mu m$. Use an NWELL layer with sheet resistance of 1760 Ω/square.

b) Determine the LN and LP required for approaches 2 and 3.

c) Compare the total area of each approach, and understand why long skinny MOSFETs are usually preferred over high value resistors in many applications.

d) Since the both approaches 2 and 3 are big winners compared to approach 1, let’s look for another reason to choose between approaches 2 and 3. Suppose there is change in temperature that changes mobilities and threshold voltages. Which approach will be better for providing a stable VMID?
2) [Op-amp DC analysis]

Figure 5-2 below shows a two-stage, low-power op-amp. Assume the op-amp is connected so that $V_{\text{in1}}$, $V_{\text{in2}}$, and $V_{\text{out}}$ all equal +2.5V, and all MOSFETs are in the saturation operating region. You may assume that the body is tied to the source for all devices (ignore the body effect). For the MOSFET parameters, use the following:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N-channel</th>
<th>P-channel</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$</td>
<td>+0.90 V</td>
<td>-0.80 V</td>
<td>V</td>
</tr>
<tr>
<td>$\mu C_{ox}$</td>
<td>6.0E-5 A/V$^2$</td>
<td>2.0E-5 A/V$^2$</td>
<td>A/V$^2$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.02 V$^{-1}$</td>
<td>0.05 V$^{-1}$</td>
<td>V$^{-1}$</td>
</tr>
</tbody>
</table>

![Figure 5-2.](image_url)
a) Find the DC operating point (drain current $I_D$ [to an accuracy of ±10%] and gate-source voltage $V_{GS}$ [to an accuracy of ±0.01V]) for all MOSFETs.

b) Identify the inverting and non-inverting inputs.

c) Find the maximum and minimum input common-mode voltage range for all MOSFETs to be in the saturation region.

d) Find the maximum and minimum output for all MOSFETs to be in the saturation region.

e) Determine the unity gain frequency (gain bandwidth product) $f_T$ for this op-amp.

f) Determine the slew rate of this op-amp.

3) [Op-amp AC analysis]

The simplified small signal model for the op-amp of the previous problem is:

![Op-amp AC analysis diagram]

a) Determine values for $g_m$, $R_o$, and $C$ of each stage. Don’t forget Miller multiplication of $C_C$ to get the equivalent value at $C_I$.

b) What is the numerical value of the DC open-loop gain $A_O$?

c) Using graph paper sketch the open-loop gain Bode plot (magnitude and phase). Be sure to label your axes and any interesting points on your plot.

d) If this op-amp is configured with negative feedback for closed-loop gain of unity, what will the phase margin be? Indicate this on your plot from (c).

e) If this op-amp is configured with negative feedback for closed-loop gain of unity, would it be stable or unstable? Explain!
4)  [Effect of design changes]

This problem concerns changes in the design parameters of the op-amp in Figure 5-2.

For parts (a) and (b), the length of devices M1 and M2 in the input differential pair are each doubled, so the new size is $15/4$; all other values remain unchanged.

a) Suppose that the length of M1 and M2 is doubled. Will the op-amp gain-bandwidth product (unity gain frequency $\omega_T$) increase, decrease, or remain the same? Explain!

b) Suppose that the length of M1 and M2 is doubled. Will the op-amp slew rate increase, decrease, or remain the same? Explain!

For parts (c) and (d), the value of $C_C$ is decreased; all other values remain unchanged. (Use the original size for M1 and M2)

c) Suppose that the value of $C_C$ is decreased. Will the op-amp slew rate increase, decrease, or remain the same? Explain!

d) Suppose that the value of $C_C$ is decreased. Will the op-amp output voltage range increase, decrease, or remain the same? Explain!

5)  10.1  (Razavi p. 373)  [Phase margin analysis]

This problem approaches the stability / phase margin problem from a gain point of view: given the pole frequencies, what is the maximum gain while maintaining an acceptable ($60^\circ$) phase margin?

6)  10.3  (Razavi p. 373)  [Phase margin analysis]
Figure 5-7 shows the differential pair input stage of an op-amp. You may assume that M1 and M2 are operating in the saturation region. The original design called for M1 and M2 to be sized identically at 100/2. Due to an imperfection in the mask used in IC fabrication, however, the actual sizes are as shown.

Determine the offset voltage \( V_{\text{OS}} \) caused by this size mismatch. That is, determine the input differential voltage \( V_{\text{id}} = V_{\text{OS}} \) required to balance the output currents so that \( I_{D1} = I_{D2} \).