ECE4902 Lecture 7

Common Source with Active Load
  Design Example

Bandwidth (6.2)
  Miller Effect

Differential Pair

Hand In:
HW 3

Handouts:
  Design Example
  Transfer Function: Poles & Nodes
  Miller Effect
  3 Cases of Differential Pair
  Bartlett’s Bisection Theorem
  Lab 7 Differential Pair Circuits
Design example: common source amplifier with active load

Determine input DC bias and value of $R_B$ required for $V_{OUT}$ DC bias of 2.5V and DC drain current of 100μA

For $M_3$: Assume Active SG Law

$$V_{GS3} = -1.5V + \sqrt{\frac{100mA}{1.125}} \times \frac{2}{2.5E-6} \times \frac{2}{900} \pm 0.89V \text{ choose - for PMOS}$$

$$V_{GS3} = -1.5V - 0.89V = -2.39V$$

KVL to gates of mirror:

$$V_{DD} + V_{GS3} = V_{G2} = 5V + (-2.39V) = 2.61V$$

$V_{DS2} \neq V_{DS3}$  $I_{D2}, I_{D3}$ a little different (channel length mod)

Ignore for now: $I_{D2} = I_{D3} = 100mA$

$$R_B = \frac{2.61V}{100mA} = 26.1kΩ$$

Disadvantage: $I_B$ sensitive to $V_{DD}$ change (solve with bias block, Bandgap $V_{REF}$)

Example process parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage $V_T$</td>
<td>$+1.50$</td>
<td>$-1.50$</td>
<td>V</td>
</tr>
<tr>
<td>Mobility- $C_{ox}$ product $\mu C_{ox}$</td>
<td>$7.0 \times 10^{-6}$</td>
<td>$2.5 \times 10^{-6}$</td>
<td>A/V²</td>
</tr>
<tr>
<td>Channel length modulation $\lambda$</td>
<td>$0.03$</td>
<td>$0.05$</td>
<td>V⁻¹</td>
</tr>
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small signal gain

\[ g_{m1} = \frac{2I_{D1}}{(V_{GS1} - V_{TH})} \]

\[ = \frac{2 \times 100 \text{mA}}{0.871} \]

\[ = 230 \text{mA/V} \]

\[ R_{o1} = \frac{1}{\lambda_1 I_{D1}} \]

\[ = \frac{1}{(0.03)(100 \text{mA})} \]

\[ = 330 \text{k}\Omega \]

\[ R_{o3} = \frac{1}{(0.05)(100 \text{mA})} \]

\[ = 200 \text{k}\Omega \]

\[ R_{out} = R_{o1}/R_{o3} = 125 \text{k}\Omega \]

\[ \frac{V_{out}}{V_{in}} = -g_{m1}R_{out} = -\left(\frac{230 \text{mA}}{125 \text{k}\Omega}\right) = -29 \Rightarrow -120 \]

\[ \Rightarrow \frac{2}{(\lambda_1 + \lambda_3)(V_{GS} - V_{TH})} \]

LARGE \( V_{GS} - V_{TH} \)

FIX: SMALLER \( (V_{GS} - V_{TH}) \) \Rightarrow 0.22
Transfer function: Poles associated with circuit nodes

Cascade of noninteracting blocks

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \left( \frac{V_{\text{out}}}{V_{2}} \right) \left( \frac{V_{2}}{V_{1}} \right) \left( \frac{V_{1}}{V_{\text{in}}} \right)
\]

PRODUCT OF INDIVIDUAL BLOCK TRANSFER FUNCTIONS!

![Diagram of cascaded amplifiers](image)

**Figure 6.6** Cascade of amplifiers.

\[
\frac{V_{1}}{V_{\text{in}}} = \left( \frac{1}{1+sR_{S}C_{\text{in}}} \right) A_{1}
\]

\[
\frac{V_{2}}{V_{1}} = \left( \frac{1}{1+sR_{1}C_{N}} \right) A_{2}
\]

\[
\frac{V_{\text{out}}}{V_{2}} = \left( \frac{1}{1+sR_{2}C_{P}} \right)
\]

**Each pole of** \( \frac{V_{\text{out}}}{V_{\text{in}}} \) **transfer function**

ASSOCIATED WITH NODE IN THE PHYSICAL CIRCUIT

**Dominant pole**

Determines bandwidth

-20 dB/Decade

-40 dB/Dec

-60 dB/Dec
Miller effect

**EE4902 MILLER EFFECT**

Consider any amplifier (not necessarily an op-amp) with gain $A$, and some impedance $Z$ from input to output. What impedance does it "look like"?

![Diagram of amplifier with input $V_x$, output $A V_x$, and impedance $Z$ between input and output.]

\[ i_x = \frac{V_x - A V_x}{Z} \]

\[ V_x = \frac{Z}{i_x} \left(1 - A\right) \]

Impedance is reduced by factor $(1 - A)$

**EXAMPLE:** $Z = 10 \Omega$ resistor

$A = -9$, $V_x = 1V$

\[ I = \frac{1V - (-9V)}{10\Omega} = 1A \]

Applying 1V causes 1A to flow: source "sees" a 10Ω resistor!

$1\Omega = \frac{10\Omega}{1 - [-9]}$

**WHEN $Z$ IS A CAPACITANCE:** $Z = \frac{1}{j\omega C}$

\[ \frac{V_x}{i_x} = \frac{1}{j\omega (1 - A) C} \]

Apparent value of C **multiplied by** $(1 - A)$!

LARGE INCREASE WHEN $A$ IS INVERTING GAIN
Miller effect in common source stage

IF $C_{DB}$ DOMINATES

$$BW = \frac{1}{2\pi R_D C_{DB}}$$

PARASITICS

IF $C_{gs}$ DOMINATES

$$BW = \frac{1}{2\pi R_S C_{gs}}$$

Figure 6.10  High-frequency model of a common-source stage.
Differential pair motivation:

1) Op-amp input

\[ V_{out} = A(V_+ - V_-) \]

SINGLE-ENDED OUTPUT
DIFERENCE OF 2 VOLTAGES

2) DC bias of common source amplifier

FORCE ANOTHER MOSFET TO CARRY \( I_D \)

NICE: \( V_{in} \)
GROUND REF'D

NOW THE CORRECT \( V_{GS} \) FOR \( I_D \)

\( \frac{W_2}{L_2} = \frac{W_1}{L_1} \)
DIFFERENTIAL PAIR

\[ V_{\text{DD}} \]

\[ I_{D1} \]
\[ V_{01} \]
\[ M_1 \]
\[ M_2 \]
\[ V_{02} \]
\[ I_{D2} \]
\[ V_{\text{in1}} \]
\[ V_{\text{in2}} \]

\[ I_{\text{BIAS}} = 2I_D \]

Output voltages:

\[ V_{01} = V_{\text{DD}} - I_{D1}R_D \quad V_{02} = V_{\text{DD}} - I_{D2}R_D \]
Building up differential amplifier characteristic

\[ I_{D1} = 0 \quad I_{D2} = I_{SS} \]

Assume drain voltages \( V_{D1}, V_{D2} \) OK for active region

\[ M_1 = M_2 \quad \text{IDENTICAL} \]

\[ I_{SS} \]

\[ I_{D1} = I_{SS} \quad O = I_{D2} \]

\[ V_+ \quad V_- \]

Connection: \( V_{GS1} = V_{GS2} \)

\[ I_{D1} = I_{D2} \]

KCL at \( S \): \( I_{D1} + I_{D2} = I_{SS} \)

KVL: \( V_{IN} - V_{GS1} + V_{GS2} = 0 \)

\[ V_{IN} = V_{GS1} - V_{GS2} \]

\[ I_{D1} \uparrow \quad I_{D2} \downarrow \]

\[ V_{O1} \quad V_{O2} \]

\[ V_{D1} - I_{SS} R_0 \]

\[ V_{D2} - I_{SS} R_0 \]
Differential Output Voltage

\[ V_{od} \]
\[ V_{o1} - V_{o2} \]

+\[ I_{ss} R_0 \]

Slope is small signal gain \[ \frac{V_{od}}{V_{id}} = -g_{m} R_0 \]

Steepest slope (max gain) for small signals

Most linear part

Zero in \[ \rightarrow \] zero out

\[ V_{+} - V_{-} \]
\[ V_{o1} - V_{o2} \]

Soft, symmetric clipping

\[ -I_{ss} R_0 \]
BARTLETT'S BISECTION THEOREM

Analysis using symmetry - "half circuit"

Consider two completely symmetrical circuits; a, b, c are connected points of symmetry

COMMON MODE

If \( v_1 = v_2 = v_c \) (both circuits have the same input; symmetric excitation) \( \Rightarrow \) then we can open all leads between points of symmetry without affecting circuit operation; no current flows across any connection

EXAMPLE: \( i = 0 \) (no voltage drop across \( R_s \) due to symmetrical excitation. We can open this connection without affecting performance

DIFFERENTIAL MODE

If \( v_1 = -v_2 \) (antisymmetric excitation) \( \Rightarrow \) then we can signal ground all leads between points of symmetry

EXAMPLE: by voltage divider, \( V_x = 0 \) regardless of \( V_d \). Therefore we can signal ground this connection without affecting circuit performance
Any two signals can be expressed in terms of common mode, differential mode

Consider any $V_1, V_2$:

\[ V_1 = V_2 - V_d \]
\[ V_d = \frac{V_1 + V_2}{2} \]

Define $V_c = \frac{V_1 + V_2}{2}$

Straightforward to verify that
\[ V_1 = V_c - \frac{V_d}{2} \]
\[ V_2 = V_c + \frac{V_d}{2} \]

Key: analyze differential amplifier by decomposing inputs into $V_c$ and $V_d$, then using symmetry (Bartlett's bisection theorem) and superposition

![Diagram](image-url)
REDRAW FOR SPLIT

M1 (U1) 5
M2 (U1) 12
CD4007

VDD = +5V
RD1 20kΩ
RD2 20kΩ
Vo1 ID1 ID2 Vo2

M3 (U2) 6
CD4007

VSS = -5V
M4 (U2) 4

RD = V01 Vo2
V01 = VDD
V02 = -VDD

\[ \text{ COMMON MODE} \]
\[ V_{CM} \]
\[ \frac{I_{SS}}{2} \]

\[ \text{ DIFFERENTIAL MODE} \]
\[ \text{(small signal)} \]

\[ \frac{V_{id}}{2} \]
\[ \frac{V_{gs}}{G_{m} V_{gs}} \]
\[ \frac{V_{o}}{R_{D}} \]

\[ \text{ DC BIAS:} \]
\[ I_{D1} = \frac{I_{SS}}{2} \]

\[ V_{o(cm)} = V_{DD} - \frac{I_{SS} R_{D}}{2} \]

\[ \frac{V_{o1}}{2} = -g_{m} R_{D} \]
\[ \frac{V_{o1}}{V_{id}/2} \]
\[ = \text{ same as CS amplifier} \]