ECE4902 Lecture 9

2-Stage Op-Amp
   1st-2nd Stage: NMOS or PMOS?!?
   DC Analysis
   Input Common-Mode Range
   Feedback
   Stability

Handouts:

Lab 8/9 Review Slides

Differential Pair
2nd Stage Common Source
Lab 8 Op-Amp

THE MOST IMPORTANT LECTURE OF ECE4902!
YOUR LIFE
Differential Pair with Mirror Load: Single Ended Output; Recovering "Other" Half of Differential Signal

**Signal:** \( V_{id} = V_{i1} - V_{i2} \)

**Symmetry:** Half at each input

\[ M_1: \frac{V_{id}}{2} \Rightarrow I_{D1} \uparrow \] \[ M_2: \frac{-V_{id}}{2} \Rightarrow I_{D2} \downarrow \]

What about \( M_3, M_4 \) mirror?

\[ M_3: \text{same as } M_1 \quad I_{D1} \]
\[ M_4: \text{mirror } I_{D3} \text{ to } I_{D4} \]

KCL "disagreement" at \( V_{out} \) node!

Difference \( i_{out} \) flows in \( Z_L \) at load

\[ \text{KCL}: \frac{I_S}{2} + g_m \frac{V_{id}}{2} = \frac{I_S}{2} - g_m \frac{V_{id}}{2} + i_{out} \]

\[ g_m V_{id} = i_{out} \]

Recover "other" half

\[ V_{out} = i_{out} Z_L = g_m V_{id} Z_L \quad \Rightarrow \quad \frac{V_{out}}{V_{id}} = g_m Z_L \]
Differential Pair with Mirror Load: Small Signal Model

\[ V_{DD} = +5V \]

**TRANSCONDUCTANCE OF DIFF PAIR**

\[ V_{id} \quad g_m V_{id} \]

**LOOKING INTO DRAIN OF M4**

**LOOKING INTO DRAIN OF M2**

\[ \frac{2I_D^2}{3} \frac{Is}{2} \]

\[ (V_{GS1} - V_{TH}) \]

\[ R_{out} = R_{o2} || R_{o4} \]

\[ = \frac{1}{(\lambda_2 + \lambda_4) I_D} \]

\[ \frac{V_{out}}{V_{id}} = \frac{g_m R_{out}}{1 + s R_{out} C_L} \]

\[ f_{3dB} = \frac{1}{2\pi R_{out} C_L} \]

\[ f_T = \frac{g_m}{2\pi R_{out} C_L} \]
2nd Stage Common Source Amplifier: NMOS or PMOS?

**Common Source with Active Load**

- **$V_{DD} = +5V$**
- **$V_{SS} = -5V$**

Diagram:

- **M3**, **M4**, **M1**, **M2**
- **$V_{GS3}$**, **$V_{GS3}^{-}$**, **$V_{GS3}^{+}$**, **$V_{TH}$**
- **$R_B$**
- **$I_s/2$**
- **$I_s$**
- **$V_{OUT}$**

- DC BIAS:
  - **$+3V$**
  - **$+1V$**
  - **$+2V$**

- **$I_{DS}$** BIG

- **NEED THIS TO BE IN ACTIVE REGION**
  - **TRIODE CRASH!**
  - **-5V to +2V**

- **WANT HIGH GAIN:**
  - **$\Rightarrow$ HIGH $g_{MS}$**
  - **$g_{MS} = \frac{2I_{DS}}{(V_{GS3} - V_{TH})}$**

- **8V!?**
2nd Stage Common Source Amplifier: NMOS or PMOS? FOR COMMON SOURCE?

\[ V_{DD} = +5V \]

\[ V_{SS} = -5V \]

\[ V_{OUT} \]

\[ V_{G5} \]

\[ (V_{G5} - V_{TH}) \]

\[ \sim 0.3, 0.4 \text{V} \]

DC BIAS \[ \approx +3 \text{V} \]

\[ g_{MS} = \frac{2I_{DS}}{V_{G5} - V_{TH}} \]

\(< 1 \text{V}\]

\[ \text{CURRENT SOURCE } \checkmark \]

\[ \text{ACTIVE LOAD } \checkmark \]

\[ \text{SWING CLOSE TO } + \text{RAIL } \checkmark \]

\[ \text{TO } + \text{RAIL} \]

\[ \checkmark \]
Lab 8 op-amp:

**INPUT STAGE**

- M3: Mirror load
- V_{DD} = +5V
- V_{G3}

**2ND STAGE**

- M4: Common source
- M5
- C_{COMP}
- V_{G5}
- V_{SS} = -5V

**V_{DD} = +5V**

- M1: Differential pair
- M2
- V_{G1}
- V_{S1}
- V_{SS} = -5V

**DIODE CONNECTED MOSFET**

- M6
- M7
- M8: Active load
- V_{G6} "Bias rail"
- I_{bias} source for diff pair

- C_{BP1} ≈ 0.01 μF
- C_{BP2} ≈ 0.01 μF

- All P: 900 / 10
- All N: 350 / 10

- R_{B}: 150kΩ
Op-amp DC Operating Point Analysis

\[ V_{DD} = +5V \]

\[ V_{OUT} \]

\[ V_{SS} = -5V \]

Strategy: Follow current around
Start: \[ I_B \] in bias for mirror
Ohm's Law for \[ R_B \]:
\[ +5V - I_B R_B - V_{G56} = -5V \]
\[ I_B = \frac{10V - V_{G56}}{R_B} \] SQU LAW \[ I_{D6} = I_B \]

Need \( \pm 20\% \)
Guess for \[ V_{G56} = 2.5V \] ?!
Try \[ \frac{10V - 2.5V}{150k\Omega} = 50\,\text{mA} \]

Check in Square Law:
\[ 50\,\text{mA} = \frac{2.6E-5}{2} \frac{350}{10} (V_{G56} - 1.9\,\text{V})^2 \]
\[ \Rightarrow V_{G56} = 2.23\,\text{V} \]

Revise \[ I_B \]
\[ \frac{10V - 2.23V}{150k\Omega} = 51\,\text{mA} \]

\[ I_{D1} + I_{D2} = I_{D7} = 50\,\text{mA} \]

\[ I_{D6} \rightarrow I_{D7}, I_{D8} \rightarrow I_{D5} = 50\,\text{mA} \]
(with negative feedback)

\[ I_{D1} = I_{D2} = 25\,\text{mA} \]
\[ M_3 = 25\,\text{mA} \rightarrow M_4: I_{D4} = 25\,\text{mA} \]

\[ I_{D3} \]

\[ V_{G56} \] values from Square Law
Labs 8 & 9 Review

• Operational Amplifier
  – Stability
  – Compensation
  – Miller Effect
  – Phase Margin
  – Unity Gain Frequency
  – Slew Rate Limiting

• Reading: Razavi ch. 9, 10
  – Lab 8, 9 op-amp is Fig. 10.34 in sec. 10.5.1
  – (see also Johns & Martin sec 5.2 pp. 232-242)
Two-stage op-amp

V_{DD} = +5V

All P: $\frac{900}{10}$
All N: $\frac{350}{10}$

M3 \hspace{1cm} M4

M1 \hspace{1cm} M2

V_{G3}

V_{in1}

V_{in2}

V_{S1}

M6 \hspace{1cm} M7 \hspace{1cm} M8

V_{G6}

R_B \approx 150k\Omega

50\mu A

V_{SS} = -5V

V_{out}

DC_BIAS

MIRROR

DIFF_PAR

CS
Analysis Strategy

- Recognize sub-blocks
- Represent as cascade of simple stages
Total op-amp model

Input differential pair

Common source stage

\[ g_{m1} = \frac{2I_{D1}}{(V_{G51} - V_{TH1})} \]

\[ g_{m2} = \frac{2I_{DS}}{(V_{G5} - V_{TH5})} \]

\[ r_{o2} || r_{o4} = \frac{1}{(\lambda_2 + \lambda_4) I_{n1}} \]

\[ r_{o5} || r_{o8} = \frac{1}{(\lambda_5 + \lambda_8) I_{DS}} \]
## DC operating point

<table>
<thead>
<tr>
<th></th>
<th>$I_D[\mu A]$</th>
<th>$V_{GS-V_{TH}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>25</td>
<td>0.235</td>
</tr>
<tr>
<td>M2</td>
<td>25</td>
<td>0.235</td>
</tr>
<tr>
<td>M3</td>
<td>25</td>
<td>0.247</td>
</tr>
<tr>
<td>M4</td>
<td>25</td>
<td>0.247</td>
</tr>
<tr>
<td>M5</td>
<td>50</td>
<td>0.350</td>
</tr>
<tr>
<td>M6</td>
<td>50</td>
<td>0.332</td>
</tr>
<tr>
<td>M7</td>
<td>50</td>
<td>0.332</td>
</tr>
<tr>
<td>M8</td>
<td>50</td>
<td>0.332</td>
</tr>
</tbody>
</table>
Small signal parameters

<table>
<thead>
<tr>
<th></th>
<th>$I_D$[μA]</th>
<th>$V_{GS}-V_{TH}$</th>
<th>$g_m$[μA/V]</th>
<th>$r_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>25</td>
<td>0.235</td>
<td>208</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>25</td>
<td>0.235</td>
<td></td>
<td>800kΩ</td>
</tr>
<tr>
<td>M3</td>
<td>25</td>
<td>0.247</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>25</td>
<td>0.247</td>
<td></td>
<td>1.43MΩ</td>
</tr>
<tr>
<td>M5</td>
<td>50</td>
<td>0.350</td>
<td>285</td>
<td>715kΩ</td>
</tr>
<tr>
<td>M6</td>
<td>50</td>
<td>0.332</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M7</td>
<td>50</td>
<td>0.332</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M8</td>
<td>50</td>
<td>0.332</td>
<td></td>
<td>400kΩ</td>
</tr>
</tbody>
</table>

Note: $\lambda_n = 0.050$ V$^{-1}$; $\lambda_p = 0.028$ V$^{-1}$
Total op-amp model: Low frequency gain

Input differential pair

\[ a_{v1} = g_{m1}(r_{O2}||r_{O4}) \]
\[ a_{v1} = (208 \mu A/V)(800k\Omega||1.43M\Omega) \]
\[ a_{v1} = 106 \]

Common source stage

\[ a_{v2} = g_{m2}(r_{O5}||r_{O8}) \]
\[ a_{v2} = (285 \mu A/V)(400k\Omega||715k\Omega) \]
\[ a_{v2} = 73 \]

\[ \frac{V_{out}}{V_{in}} \sim 7000 \]
Total op-amp model with capacitances

Gate of M5

Load: scope probe $\approx 10\text{pF}$

$$C_g = (900 \mu \text{m})(10 \mu \text{m}) \left(4.17 \times 10^4 - 4 \frac{F}{m^2}\right)$$

$$C_g = 3.74 \text{pF}$$

EACH CAP: 1 POLE TO TRANSFER FUNCTION $\frac{V_{\text{out}}(f)}{V_{\text{in}}}$

ONLY 2 HIGH IMPEDANCE NODES: $V_{\text{gs}}$, $V_{\text{out}}$

DOMINANT POLE
Total op-amp model with capacitances

First stage pole

\[ f_{p1} = \frac{1}{2\pi \left( r_{O2} || r_{O4} \right) C_{g5}} \]

\[ f_{p1} = \frac{1}{2\pi \left( 800k\Omega || 1.43M\Omega \right) (3.74 \text{ pF})} \]

\[ f_{p1} = 82\text{ kHz} \]

Second stage pole

\[ f_{p1} = \frac{1}{2\pi \left( r_{O5} || r_{O8} \right) C_L} \]

\[ f_{p1} = \frac{1}{2\pi \left( 400k\Omega || 715k\Omega \right) (10 \text{ pF})} \]

\[ f_{p1} = 61\text{ kHz} \]
Open loop transfer function

• Product of individual stage transfer functions

\[ A(j\omega) = \frac{g_{m1}(r_{o2}||r_{o4})g_{m5}(r_{o5}||r_{o8})}{\left[1 + j\omega(r_{o2}||r_{o4})C_g\right]\left[1 + j\omega(r_{o5}||r_{o8})C_L\right]} \]

• Numerically (using \( \omega = 2\pi f \))

\[ A(j\omega) = \frac{7738}{\left[1 + j\left(\frac{f}{82kHz}\right)\right]\left[1 + j\left(\frac{f}{61kHz}\right)\right]} \]

• Check Bode plot simulation; predicts:
  – DC gain = 20log(7738) = +78dB
  – Unity gain frequency ~ 6.2 MHz

\( \text{SET} |A(\omega)| = 1 \)
Two-stage op-amp: Simulation Schematic

C_L = 10pF

In M" Mρ models

Only parasitics
DC Operating Point Simulation

DC Response

OP POINT 2.885 mV

Systematic Offset!

IF WE DIDN'T:
MUCH SMALLER GAIN!

NEED THIS $V_{IN\,(DC)}$

$7700 \neq 5000$

$A_L$ LARGE

DC OFFSET $\{V_+\}
Bode plot

- Magnitude, phase on log scales
- Pole: Root of denominator polynomial
Open loop Bode plot

- Product of terms: Sum on log-log plot

20 log (DC Gain) → $|A|$

-20 dB/dec

-40 dB/dec

$\angle A$

-90°

-180°
Open Loop Bode Plot Simulation

Note: AC source at input also needs DC component to account for systematic offset!
Check Open Loop Bode Plot Simulation

$\sqrt{\text{DC gain}} \sim +78\text{dB}$

Unity gain $\sim 16\text{MHz}$

A: (15.592M 36.0461m)  delta: (255.918K  -195.979)  slope:  -768.698u
Stability example: Closed loop follower

- **Negative feedback:** Output connected to inverting input
- **Gain should be ~ 1**

\[
v_{out} = A(v_{in} - v_{out})
\]
\[
v_{out}(A + 1) = Av_{in}
\]
\[
v_{out} = \left(\frac{A}{A + 1}\right) v_{in}
\]
\[
\approx 1 \text{ as } A \gg 1
\]
Unity gain: Why bother?

- **No buffer:**
  Voltage divider
- **Signal reduced due to voltage drop across** $R_S$

- **With buffer:**
  No current required from source

\[
\begin{align*}
  v_{out} &= \left(\frac{R_L}{R_L + R_S}\right) v_{in} \\
  v_{out} &= v_{in}
\end{align*}
\]
Lab 9 Problem: Instability

- Oscillation superimposed on desired output!?!
Lab 9 Problem: Instability

- Ground $v_{in}$: Output for zero input?!?
- Why? Need...

For this waveform, $\frac{V_{out}}{V_{in}} = 0.0$
Controls: ECE3012 in 20 minutes

• General framework
  A: Forward Gain
  β: Feedback Factor
  fraction of output fed back to input
Example: Op-amp, Noninverting Gain

**A: Forward Gain**

Op-amp open loop gain

\[ V_{out} = A(V_+ - V_-) \]

Transfer function \( A(j\omega) \)

**\( \beta \): Feedback Factor**

\[ \beta = \frac{R_1}{R_1 + R_2} \]

VOLTAGE DIVIDER
Closed Loop Gain

- **Output**
  \[ v_{out} = A \left( v_{in} - \beta v_{out} \right) \]
  \[ v_{out} = v_{+} - v_{-} \]

- **Solve for** \( \frac{v_{out}}{v_{in}} \)
  \[ v_{out} = Av_{in} - A\beta v_{out} \]
  \[ (1 + A\beta)v_{out} = Av_{in} \]
  \[ \frac{v_{out}}{v_{in}} = \frac{A}{1 + A\beta} \]
Op-amp with negative feedback

• If $A\beta \gg 1$

\[
\frac{v_{out}}{v_{in}} \approx \frac{A}{1 + A\beta} \Rightarrow \frac{v_{out}}{v_{in}} \approx \frac{1}{\beta}
\]

• Closed loop gain determined only by $\beta$

• Advantage of negative feedback:
Open loop gain $A$ can be ugly (nonlinear, poorly controlled) as long as it's large!
Example: Op-amp, Noninverting Gain

\[ \beta: \text{Feedback Factor} \]

\[ \beta = \frac{R_1}{R_1 + R_2} \]

Closed loop gain

\[ \frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1} = \frac{1}{\beta} \]
Reexamine closed loop transfer function

- Output with no input: infinite gain
  \[ \frac{v_{out}}{v_{in}} = \infty \]
- Infinite when \( 1 + A\beta = 0 \)
- Condition for oscillation:
  \[ 1 + A\beta = 0 \]
- In general \( A, \beta \) functions of \( \omega \)
- If there's a frequency \( \omega \) at which \( 1 + A\beta = 0 \):
  Oscillation at that frequency!
Example: follower

\[ \beta = 1 \quad \rightarrow \quad \frac{v_{out}}{v_{in}} = \frac{A}{1 + A} \]

- Use \( A(j\omega) \), solve for \( 1 + A = 0 \)
- No thanks!

\[
A(j\omega) = \frac{g_{m1}(r_{o2}||r_{o4})g_{m5}(r_{o5}||r_{o8})}{1 + j\omega(r_{o2}||r_{o4})C_{g5}} \left[ 1 + j\omega(r_{o5}||r_{o8})C_L \right]
\]
Reexamine condition for oscillation

\[ \text{DEN} \{ 1 + A\beta = 0 \rightarrow A\beta = -1 \]  

Magnitude and phase condition:  

\[ |A\beta| = 1 \ \text{AND} \ \angle A\beta = -180^\circ \]

• Easier to get from Bode plot
Look at original $A\beta$ for 2 stage op-amp

- Find $\omega$ at which $|A\beta| = 1$; Check $\angle A\beta -180^\circ$ ?

Trouble!
Simulation Aβ for 2 stage op-amp

Unity loop gain at ~ 16MHz

> 180° phase lag at unity loop gain!

• Causes closed-loop instability
Compensation: “Dominant Pole”

- Move one pole to lower frequency
- How?

Move unity loop gain frequency $f_T$ to lower value

So accumulated phase lag at $f_T$ hasn’t reached -180°
Compensation: “Dominant Pole”

• Need to increase capacitance by $\approx 1000X$:
  
  BAD! Die area cost
Miller Effect

- Impedance across inverting gain stage $G$
- Reduced by factor equal to $(1+G)$

\[ \frac{1}{(1+G)C} = C_{eq} \]
Math for Miller effect:

\[ i_x = \frac{v_x - (-Gv_x)}{Z} \]

\[ i_x = \frac{v_x(1 + G)}{Z} \]

\[ \frac{v_x}{i_x} = Z_{in} = \frac{Z}{(1 + G)} \]

- Impedance across inverting gain stage G
- Reduced by factor equal to (1+G)
Example: Impedance is capacitive

- Capacitance multiplied by (1+G)
  \[ Z_{in} = \frac{Z}{1+G} \]

- Equivalent capacitance higher by factor 1+G

\[ Z = \frac{1}{sC} \quad \rightarrow \quad Z_{in} = \frac{1}{s(1+G)C} \]

- Problem for high bandwidth amplifiers
- Opportunity for compensation ...
Miller Compensation

• Need effect of large capacitance
• Use Miller effect to multiply small on-chip capacitance to higher effective value
• Effect of large capacitance without die area cost of large capacitance
New schematic

- Add $C_C$ across 2nd stage
New loop gain transfer function

AC Response

Unity loop gain at ~65kHz

125° phase lag at unity loop gain
New step response

• No oscillation!
New step response with $C_C$

- Zoom in on small-signal step response:
  Some overshoot and ringing
Reason: RHP zero in complete transfer function

Complete transfer function looks like:

\[ A(j\omega) = A_0 \left(1 - \frac{j(\omega/\omega_z)}{1 + j(\omega/\omega_{p1})[1 + j(\omega/\omega_{p2})]} \right) \]

Effect of RHP zero: additional phase lag

Open loop gain A with only 2 poles

• See Razavi 10.5, Johns & Martin 5.2
"Phase margin"

- How stable is new transfer function?
- Phase margin = Phase lag at $|A\beta| = 1$ minus (-180°)
- Usually want at least 60° for stable step response
Phase margin of op-amp with $C_c$

Unity loop gain at ~65kHz

125° phase lag at unity loop gain

Phase margin = 55°
Solution to RHP zero problem

- Add $R_Z$ in series with $C_C$
- Moves RHP zero to much higher frequency
New step response with $R_Z, C_C$

- Zoom in on small-signal step response:
  No overshoot, ringing: phase margin improved
Large signal step response

- Slew Rate Limiting!?!?

See Solomon op-amp paper for model; rising/falling asymmetry
Dominant pole op-amp model

- Simpler model with dominant pole from $C_C$

$V_{DD}$

$V_{SS}$

$I_{BIAS}$

M1, M2

M3, M4

$C_C$

$V_{1}$

$g_{m1}V_{in}$

$V_{OUT}$

$+I_{BIAS}$

$-I_{BIAS}$

$V_{in}$

$g_{m}$

$V_{out}$

SEE FULL $V_{OUT}$ SWING

2nd STAGE

MAX CURRENT OUT OF OFF PAIR

$g_{m}$
Approximate dominant pole transfer function

\[ A(j\omega) \approx \frac{g_{m1}(r_{o2}\|r_{o4})A_2}{1 + j\omega(r_{o2}\|r_{o4})A_2C_C} \]

\[ A_2 = g_{m5}(r_{o5}\|r_{o8}) \]

Miller multiplied

2nd stage gain

0 C GAIN
Unity gain frequency

- Depends only on
  - Input stage
    transconductance $g_{m1}$
  - Compensation capacitor $C_C$

$$|A(j\omega)| \approx \frac{g_{m1}(r_{o2}\parallel r_{o4})A_2}{\omega(r_{o2}\parallel r_{o4})A_2C_C}$$

$$|A(j\omega)| = 1 \text{ at } \omega_T$$

$$\omega_T \approx \frac{g_{m1}}{C_C}$$

$$f_T = \frac{g_{m1}}{2\pi C_C}$$
Slew rate

- \( I = C \frac{dV}{dt} \)
- Only limited current \( I_{\text{BIAS}} \) available to charge, discharge \( C_C \)
Slew rate

- \( I = C \frac{dV}{dt} \Rightarrow \frac{dV}{dt} = \frac{I_{BIAS}}{C_C} \)
Summary Op-amp:

- Stability
- Compensation
- Miller effect
- Phase Margin
- Unity gain frequency
- Slew Rate Limiting