ECE4902 Lecture 12

How to Increase Open Loop Gain?

Improving Performance: Cascode Op-amp *
Tradeoff:  
+ Higher node impedance  
- Reduced signal swing

2-Stage Op-Amp
CL, Phase Margin Issue

1-stage op-amp (Johns & Martin 6.2)
Improving Performance: Cascode

* Bandgap Voltage Reference

(* Optional Lab Circuit *)

Hand In:
HW 5

Handout:
Op-Amp Slides
Cascode Op-Amp
Bandgap Voltage Reference
  Principle
  Circuit

small signal resistance at 1st stage output
2nd stage input

Gm1 = Gm5

GMI
GMI
RI
RT
SR
OUTPUT
CURRENT
REGI
CAN'T CONTROL
WHAT IS AT
OUTPUT?
Review: Small signal (ac) model of 2-stage op-amp

Identify +, - inputs: How?
Follow signal path from input → output
Count sign inversions

In this case, \( V_1 \Rightarrow V_{out} \) 3 inversions:
\( V_1 \) - input
\( V_2 \) + input (2 inversions)

Miller says: \( i_c > V_{gs} \); \( i_c \) bigger than expected from \( V_{gs} \)

\[
\frac{1}{2\pi RC}
\]

\[
\frac{1}{2\pi \left( r_{o2} || r_{o4} \right) \left( 1 + A_2 \right) C_C}
\]

Dominant pole

Output pole (nondominant) [we hope]

\[
\frac{1}{2\pi \left( r_{o5} || r_{o8} \right) C_L}
\]

\[
\frac{1}{2\pi \left( r_{o2} || r_{o4} \right) C_C}
\]
Complete transfer function, stability plot

* Increasing node impedance at 1st stage output does not affect phase margin! Separate gain, stability problems

\[ \frac{\left( r_{\text{in}} \parallel r_{\text{in}} \right)}{} \uparrow \]

\[ |A| = g_{\text{in}} \left( r_{\text{in}} \parallel r_{\text{in}} \right) g_{\text{out}} \left( r_{\text{out}} \parallel r_{\text{out}} \right) \]

\[ A_0 \]

\[ \text{NON DOMINANT POLE} \]

\[ f_T \]

\[ f_{p1} \]

\[ \frac{2\pi \left( r_{\text{in}} \parallel r_{\text{in}} \right) (1+A_2) C_c}{f_T} \]

\[ \angle A = -90^\circ - \tan^{-1} \left( \frac{f}{f_p} \right) \]

\[ \phi_m \]

\[ -180^\circ \]

\[ \text{SAME} = f_T \]

\[ \text{TO APPROXIMATE PHASE NEAR } f_T \]

\[ \text{TRY THIS ONE WEIRD TRANSFER FUNCTION TIP} \]

\[ \text{BEHAVIOR OF } |A|, \angle A \text{ NEAR } f_T \]

\[ A(f) = \frac{A_0}{(1 + j\left( \frac{f}{f_{p1}} \right))(1 + j\left( \frac{f}{f_{p2}} \right))} \]

\[ \text{MAGNITUDE} \]

\[ \sqrt{1 + \left( \frac{f}{f_{p1}} \right)^2} \sqrt{1 + \left( \frac{f}{f_{p2}} \right)^2} \]

\[ \approx 1 \text{ FOR } f \ll f_{p2} \]

\[ \frac{f}{f_{p1}} \]

\[ \text{NEAR } f_T \]

\[ |A(f)| \approx \frac{A_0}{\left( \frac{f}{f_{p1}} \right)} \]

\[ \text{AT } f_T \]

\[ |A(f_T)| = 1 \]

\[ \frac{A_0}{f_T} = 1 \Rightarrow f_T = A_0 f_{p1} \]
Cascode Current Source Development

\[ I_{out} = \frac{1}{r_{o2}} \]
\[ V_{DS2} \]
\[ R_{out} = r_{o2} = 100 \text{k}\Omega \]

"SOURCE DEGENERATION"

\[ R_{out} \text{ INCREASED} \]
\[ R_{s} \text{ AREA} \]
\[ \times \text{ HEADROOM REDUCED} \]

\[ R_{out} = r_{o2} \left(1 + g_{m4} r_{o2}\right) \approx 10 \text{ M}\Omega \checkmark \]

HEADROOM xx

PROBLEM

\[ I_{out} = I_{D2} = \frac{\mu C_{ox} W \left(V_{GS} - V_{TH}\right)^2 \left(I + \lambda V_{DS}\right)}{2 L} \]
\[ V_{DS} \uparrow \Rightarrow I_{D2} \uparrow \]

HOW TO KEEP \( I_{D2} \) FROM CHANGING?

CHANGE \( L \): \& SMALLER \checkmark ? CAN SCALE \( W \): MORE AREA \xmark NOT OK

CHANGE \( V_{GS} \)

\[ V_{DS} \uparrow \Rightarrow I_{D2} \uparrow \Rightarrow V_{GS} \downarrow \]

KVL LOOP

\[ \text{KVL: } I_{REF} r_{s} + V_{GS1} - V_{GS2} - I_{out} r_{s} = 0 \]

\[ V_{GS2} = V_{GS1} - \left(I_{out} - I_{REF}\right) r_{s} \]

NEGATIVE FEEDBACK!

\[ I_{out} \uparrow \Rightarrow V_{GS2} \downarrow \]

PROBLEM

\[ V_{OUT} \text{ CHANGED } V_{DS2} \]
\[ \Rightarrow \text{ CHANGED } I_{D2} \]
\[ \text{MAGIC: PASSES } I_{D2} \text{ THRU} \]
\[ \text{BUT KEEPS } V_{DS2} \text{ CONSTANT} ?? \]

\[ M_{4}: I_{D} = I_{S} \]

VOLTAGE? \[ V_{DS2} = V_{BIAS} - V_{GS4} \approx \text{CONSTANT} \]

\[ M_{4}: \text{"CASCADE"} \]
Current source comparison: Simulation

SAME I REF

SIMPLE MIRROR

SOURCE DEGENERATED

CASCODE

SWEEP
ID vs. V_DS SWEEP COMPARISON: SIMPLE MIRROR – SOURCE DEGENERATED – CASCODE

DC Response

SIMPLE MIRROR CRASH @ V_DS ~ 0.5V
BEST VOLTAGE RANGE
MID VOLTAGE RANGE
worst Rout
better Rout
best Rout

CASCODE CRASH @ V_DS ~ 1.3V
Worst Range

ECE4902 B2015 Lec 11 14
Cascode Op-Amp (Optional Lab 10)

Crank up to ~1mV/\text{dv} at low freq.

Original 2 stage \( A_0 = 5000 \)

\( A_2 \approx 50 \)

What is signal swing here? \( V_{\text{out}} = 5V \)

\( V_{6s} = \frac{5V}{50} = 0.1V \)

Figure 9-1
To cascode the internal node, you'll need a fourth CD4007 chip. Connect it as shown here:

\[ V_{DD} = +5V \]

\[ U4 \]

\[ M4 \]

\[ M5 \]

\[ 30k\Omega \]

\[ 20k\Omega \]

\[ \text{BIAS FOR CASCODE} \]

\[ 10 \]

\[ 12 \]

\[ V_{G5} \]

\[ \approx g_m r_{o4} r_{o4} \]

\[ r_{o4}(1 + g_m r_{o2}) \approx g_m r_{o2} r_{o2} \]

\[ M2C \]

\[ M9C \]

\[ \text{CD4007 NMOS CASCODE} \]

\[ R_{OI} = r_{o2} (r_{o2} g_m || r_{o4} r_{o4} g_m) \]

\[ \approx \text{EQUA}L \]

\[ R_{OI} \text{ INCREASED BY FACTOR OF } \frac{g_m r}{50} \]
2-Stage Op-Amp Phase Margin vs. $C_{LOAD}$

Transients Response

- $v_{out}$ (load=1.00e-11)
- $v_{out}$ (load=1.00e-10)
- $v_{out}$ (load=1.00e-09)

- $C_L = 100\, \text{pF}$: OVERSHOOT & RINGING
  - $\phi_M$: MARGINALLY STABLE

- $10\, \text{pF} \, C_L$
  - NO OVERSHOOT
  - $\phi_M \checkmark$

- $C_L \uparrow \Rightarrow f_p \downarrow$

- $|A| \uparrow \Rightarrow C_L \uparrow$

- TOO MUCH $\phi$ SHIFT FROM 2ND POLE $f_p$

- $C_{LOAD} = 10\, \text{pF}, 100\, \text{pF}, 1000\, \text{pF}$

- Phase margin $\phi_M$ degrades as $C_{LOAD}$ increases

ECE4902 B2015 Lec 12
1-Stage ("gm-C" "transconductor") Op-Amp

ALL OTHER NODES IN SIGNAL PATH:
DIODE-CONNECTED MOSFETS:
LOW IMPEDANCE $r \approx \frac{1}{g_m} \approx 1 \text{kQ}$

• Only one high impedance node: $C_{LOAD}$ compensates
1-Stage ("gm-C" "transconductor") Op-Amp

- $C_{LOAD} = 1000\,\text{pF}, 10000\,\text{pF}: \phi_M$ same as $C_{LOAD}$ \uparrow
- Unity gain frequency $f_T$ worse, but always stable
1-Stage Problem

- Lousy DC gain ≈ 90 (39 dB)
- Solution: Add cascode to high impedance node
1-Stage with Cascodes

PMOS Cascode Devices

NMOS Cascode

Cascode Mirrors

Higher $R_{out}$ due to cascodes ($\sim g_{m0}$ higher)

Cascode Current Mirrors
1-Stage with Cascodes

**MORE ACCURATE D.C. PERFORMANCE DUE TO HIGHER $A_0$**

**ONLY WORKS WITH CAPACITIVE LOAD IF $R_L$: NEED LOW OUTPUT Z OUTPUT STAGE**

- $C_{LOAD} = 1000pF, 10000pF$: $\phi_M$ same as $C_{LOAD}$ ➔ **DYNAMIC SAME**
- Unity gain frequency $f_T$ worse, but always stable
Bandgap Voltage Reference (Optional Lab 11)

Motivation: DC Bias

\[ I_{BIAS} : \text{SLEW RATE (I_{SS})} \]
\[ f_T = \frac{g_{m1}}{2\pi C_C} \]

\[ I_{BIAS} = \frac{(V_{DD} - V_{SS}) - V_{GS}}{R_{BIAS}} \]

Could change! ??
Supply!
Temperature change

⇒ Want \( I_{SS}, \) \( f_T, \) ... insensitive to supply, temp variations!
Bandgap Principle

$V_{BE}$ vs Temperature

$T = 0^\circ K$ (ABSOLUTE ZERO)

**Figure 6. Typical Base-to-Emitter Voltage Characteristic vs Temperature for Each Transistor**
Here's the bandgap circuit covered in lecture:

The CA3046 is a 5 NPN transistor array. Its data sheet is available on the course website.