Name SOLUTIONS

ECE Box # _____

A	91 - 100
B	76 - 90
C	60 - 75

μ	84.9
σ	13.5
MED	88

Problem	Average Score	Points
1	22.9	25
2	12.7	15
3	21.9	25
4	14.3	20
5	13.1	15

ECE4902 B2015

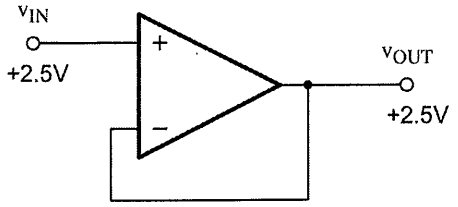
Analog IC Design

Final Exam
December 15, 2015

- This is a **closed book, closed notes test!** Use of calculators is OK, but **no pre-stored data or formulas allowed!**
- The last page is a notes page that may be detached for convenience and need not be turned in with the exam
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- **Look for the simple, straightforward way to solve the problem for the level of accuracy required. Don't get entangled in unnecessary algebra.**
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- You have one hour and 50 minutes to complete this exam. There are five problems on a total of 13 pages (including notes page).

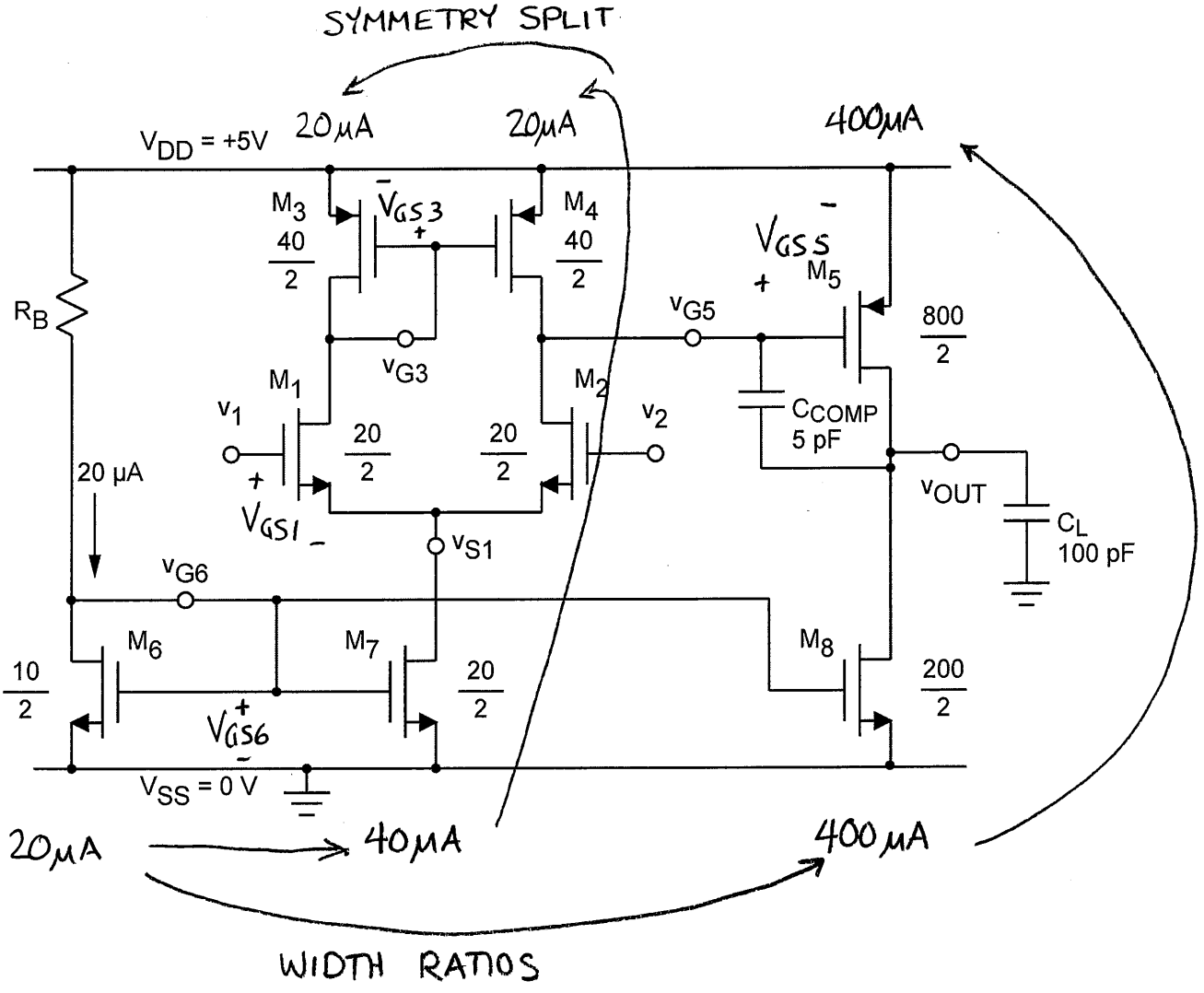
1. This problem is concerned with the op-amp circuit shown in the figure below. This op-amp is intended for single-supply applications, with supply rail voltages of V_{DD} = +5V and V_{SS} = 0V (ground). In this application, a colleague has seen that the 100pF load capacitance at the v_{OUT} node has caused slow op-amp behavior, and proposes increasing the op-amp unity-gain frequency by reducing the compsenation capacitor C_{COMP} to 5pF.

For the purposes of this problem, you may assume the op-amp is connected as a follower with with negative feedback so that all MOSFETs are in the saturation (active) region, and input and output node voltages are +2.5V.



For the MOSFET parameters, use the following:

Parameter	N-channel	P-channel	Units
V_{TH}	+0.90	-0.80	V
μC_{ox}	6.0E-5	2.0E-5	A/V^2
λ	0.02	0.05	V^{-1}



a) V_{GS} values from square law:

M_1, M_2

$$20\mu A = \frac{6E\text{-}5}{2}\,\frac{20}{2}\left(V_{GS1} - 0.9\right)^2$$

$$V_{GS1} - 0.9V = \sqrt{20\mu A\left(\frac{2}{6E\text{-}5}\right)\left(\frac{2}{20}\right)} = \underbrace{0.258}_{V_{OV1}\text{ FOR 2(a)}} \Rightarrow V_{GS1} = 1.158\,V$$

M_3, M_4

$$20\mu A = \frac{2E\text{-}5}{2}\,\frac{40}{2}\left(V_{GS3} - (-0.8)\right)^2$$

$$V_{GS3} + 0.8V = \sqrt{20\mu A\left(\frac{2}{2E\text{-}5}\right)\left(\frac{2}{40}\right)} = \underbrace{0.316}_{V_{OV5}\text{ FOR 2(c)}} \Rightarrow V_{GS3} = -1.116\,V$$

M_5 HAS SAME I_D/W RATIO; SAME V_{GS}

M_6, M_7, M_8

$$20\mu A = \frac{6E\text{-}5}{2}\,\frac{10}{2}\left(V_{GS6} - 0.9\right)^2$$

$$V_{GS6} - 0.9V = \sqrt{20\mu A\left(\frac{2}{6E\text{-}5}\right)\left(\frac{2}{10}\right)} = \underbrace{0.365}_{V_{OV6}\text{ FOR 2(c)}} \Rightarrow V_{GS6} = 1.265\,V$$

a) Find the DC operating point (drain current I_D and gate-source voltage V_{GS}) for all MOSFETs. Accuracy for currents ±20%; accuracy for voltages ±0.05V. Use the table below to record your answers.

[15]

MOSFET	Drain current I_D [μA]	Gate-Source voltage V_{GS} [V]
M1	20	1.158
M2	20	1.158
M3	20	-1.116
M4	20	-1.116
M5	400	-1.116
M6	20 μA	1.265
M7	40	1.265
M8	400	1.265

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b) Determine the voltage with respect to ground at each node. **[5]**

	Node voltage [V]	
V_1	+2.5 V	
V_2	+2.5 V	
V_{OUT}	+2.5 V	
V_{S1}	+1.34	$V_1 - V_{GS1}$
V_{G3}	+3.88	$V_{DD} + V_{GS3}$
V_{G5}	+3.88	$V_{DD} + V_{GS5}$
V_{G6}	+1.27	V_{GS6}

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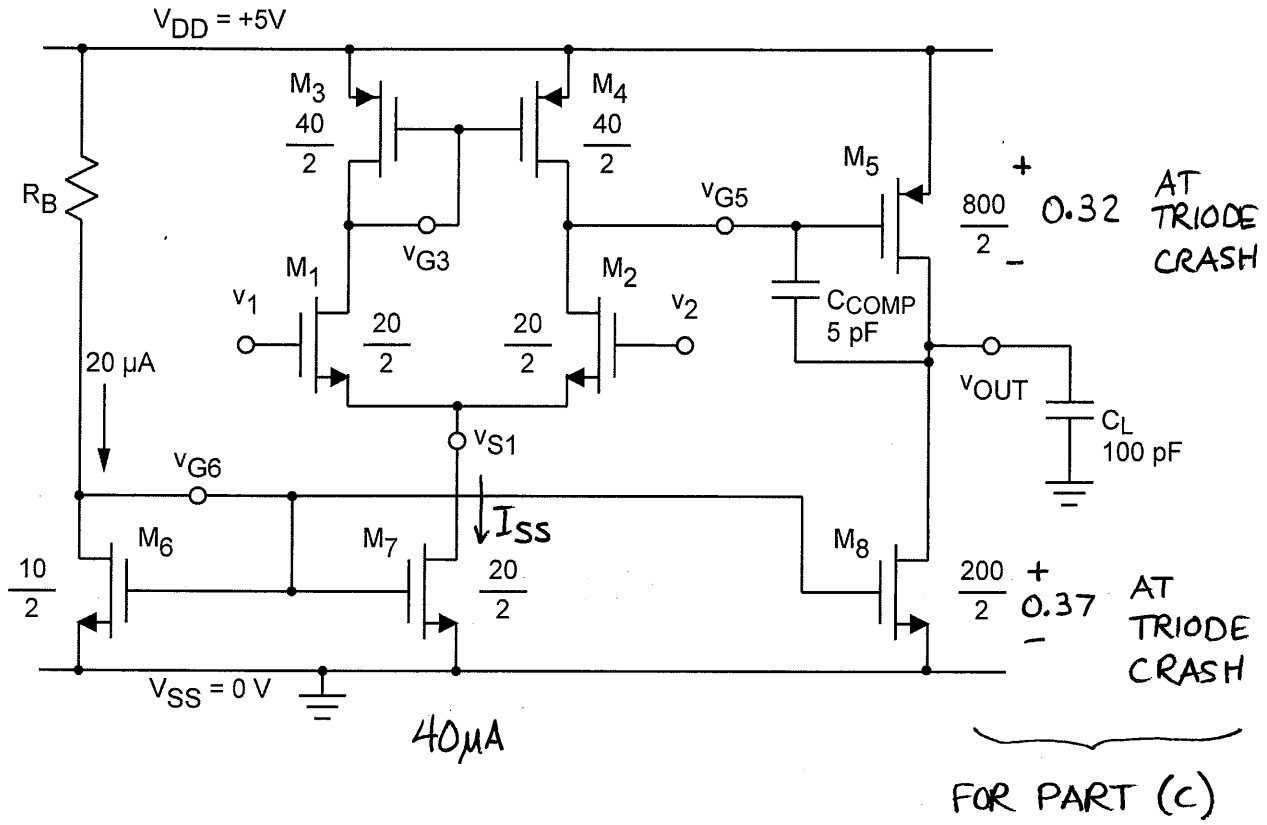
c) Determine the value of the resistor R_B. Accuracy ±20%.

[5]

R_B = 187 kΩ

OHM'S LAW $\frac{5V - 1.27V}{20\mu A}$

2. Continuing with the op-amp circuit from the previous problem, shown again in the figure below.



a) Assuming the dominant pole model, determine the expected value of the unity gain frequency (gain bandwidth product) f_T for this op-amp. Accuracy ±20%. [5]

f_T = 4.9 MHz

$\frac{g_{m1}}{2\pi C_C}$ ← $\frac{2I_{D1}}{V_{OV1}} = \frac{2(20\mu A)}{0.258V} = 154\,\mu A/V$

$\frac{154E\text{-}6}{2\pi(5\,pF)} = 4.9\ MHz$

---

b) Determine the slew rate in V/μs for this op-amp. Accuracy ±20%. [5]

SR = 8 V/µs

$\frac{I_{SS}}{C_C} = \frac{40\mu A}{5\,pF} = 8E+6\ \frac{V}{sec}$

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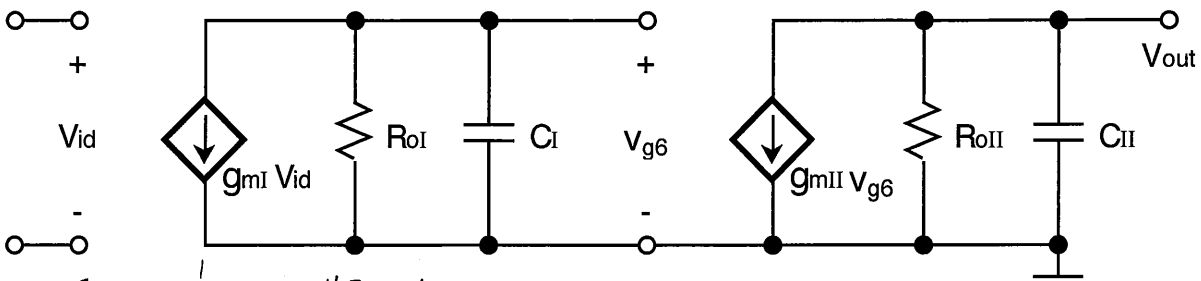
c) Determine the output voltage swing range: the minimum and maximum output voltages $V_{OUT(MIN)}$ and $V_{OUT(MAX)}$ for all MOSFETs to operate in the saturation (active) region. Accuracy ±0.05V. [5]

$V_{OUT(MIN)}$ = 0.37 $\qquad$ $V_{OUT(MAX)}$ = 4.68

0V + V_{OV6} $\qquad$ $V_{DD} + V_{OV5}$

TRIODE CRASH WHEN $V_{DS} = \underbrace{V_{GS} - V_{TH}}_{V_{OV}}$

3. The simplified small signal model for the op-amp of the previous problem is:



POLE FREQUENCIES: $\frac{1}{2\pi R_{OI} C_I} = 490\ Hz$; $45\ kHz$

STAGE DC GAINS	g_{mI}	R_{OI}	C_I	g_{mII}	R_{OII}	C_{II}
	1.54E-4 A/V	714 kΩ	455 pF	2.52E-3 A/V	35.7 kΩ	100 pF
	$A_{VI} = 110$			$A_{VII} = 90$		

a) What is the numerical value of the DC open-loop gain A_O? **[5]**

$A_O =$ 9900 +80 dB

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b) Using the graph paper on the following page, **CAREFULLY** sketch the open-loop gain Bode plot (magnitude and phase). Be sure to label your axes and any interesting points on your plot.

[6]

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c) If this op-amp is configured with negative feedback for closed-loop gain of unity, what will the phase margin be? Indicate this on your plot from (b).

[5]

Phase margin $\cong$ 5°

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d) If this op-amp is configured with negative feedback for closed-loop gain of unity, would it be stable, marginally stable, or unstable? (Circle one)

[1]

STABLE **(MARGINALLY STABLE)** **UNSTABLE**

Explain! ϕ MARGIN NEEDS TO BE > 70° TO BE STABLE (NO OVERSHOOT) **[3]**

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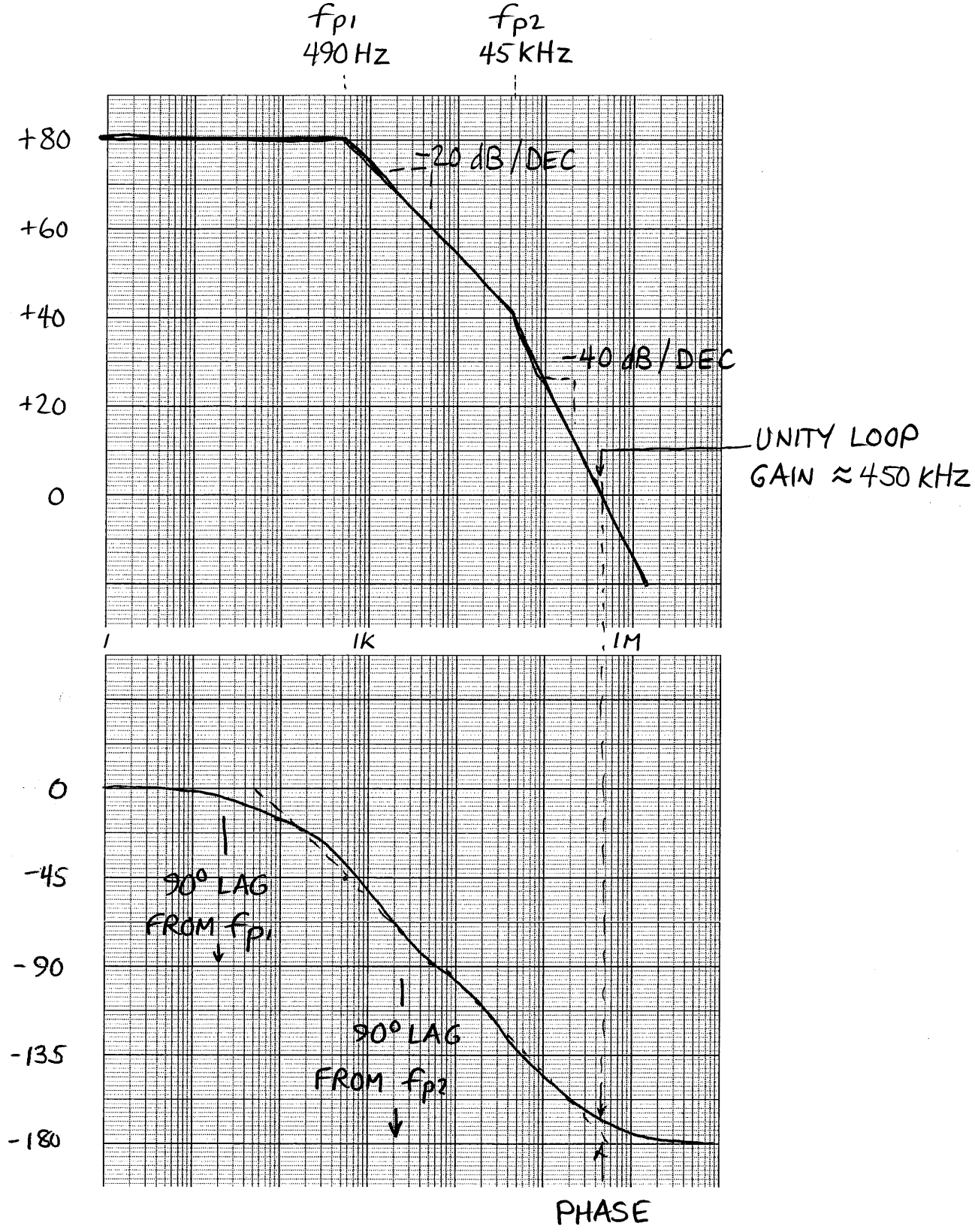
e) Why is the value of C_I in the small signal model so much bigger than C_{COMP}? Explain!

MILLER EFFECT **[5]**



PROBLEM! C_C IS TOO SMALL, DOESN'T MOVE f_{p1} TO A LOW ENOUGH FREQUENCY; f_{p2} OCCURS BEFORE UNITY LOOP GAIN FREQUENCY

4. This problem involves design of a differential amplifier, shown in schematic form on the opposite page. The amplifier is powered by split ±5V supply rails. MOSFETs M1 and M2 form the differential pair; these are identical devices with width equal to W1. Bias current of I_{BIAS} = 200μA for the differential pair is provided by the current mirror formed by MOSFETs M3 and M4; note the unequal widths W3 ≠ W4.

For this problem, you may ignore channel length modulation effects and the body effect. For the MOSFET parameters, use the following:

Parameter	N-channel	P-channel	Units
V_{TH}	+0.90	-0.80	V
μC_{ox}	6.0E-5	2.0E-5	A/V^2

a) Find the value of $R_{D1} = R_{D2} = R_D$ required for a DC bias voltage level of +2.5V at outputs v_{O1} and v_{O2} when $v_{IN} = 0$. Accuracy ±10%. **[3]**

R_D = 25KΩ DC BIAS CONDITION: $\left(\frac{I_{BIAS}}{2}\right)R_D = 5V - 2.5V$

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b) Choose R_B so the M3/M4 mirror produces I_{BIAS} = 200μA. Accuracy ±10%. **[4]**

R_B = 176KΩ OHM'S LAW

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c) Choose width W1 = W2 = W for M1 and M2 so that the small signal differential voltage gain magnitude is $|v_{od}/v_{in}| = 12$. Accuracy ±10%. **[4]**

W = 38 FOR $g_m = \frac{12}{R_D} = 480\mu A/V = \sqrt{2(100\mu A)(6E\text{-}5)\frac{W_1}{2}}$

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d) In the space on the opposite page, sketch the total v_{O1} and v_{O2} that result when the input is a low frequency sine wave with differential amplitude of 0.2V peak. Be sure to indicate any interesting information (such as peak voltage values) on your plot. **[3]**

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e) In the space on the opposite page, sketch the total v_{O1} and v_{O2} that result when the input is a low frequency sine wave with differential amplitude of 1.0V peak. Be sure to indicate any interesting information (such as peak voltage values) on your plot. **[3]**

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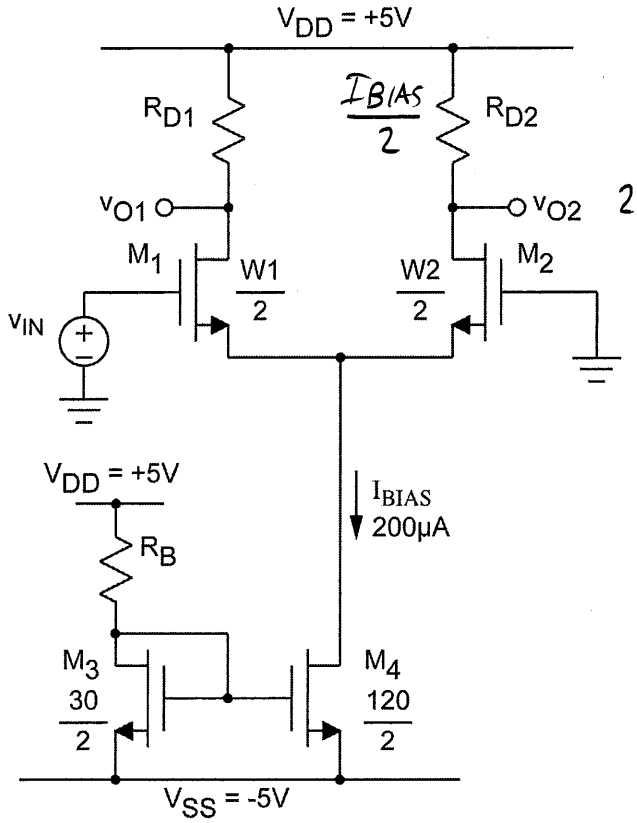
f) A colleague proposes to increase the small signal differential voltage gain magnitude (without affecting the output DC operating point), by doubling the value of W from part (c) while keeping the other design values (I_{BIAS}, R_B, R_D) unchanged. Will this work? Circle one: **[1]**

YES, IT WILL WORK **NO, IT WON'T WORK**

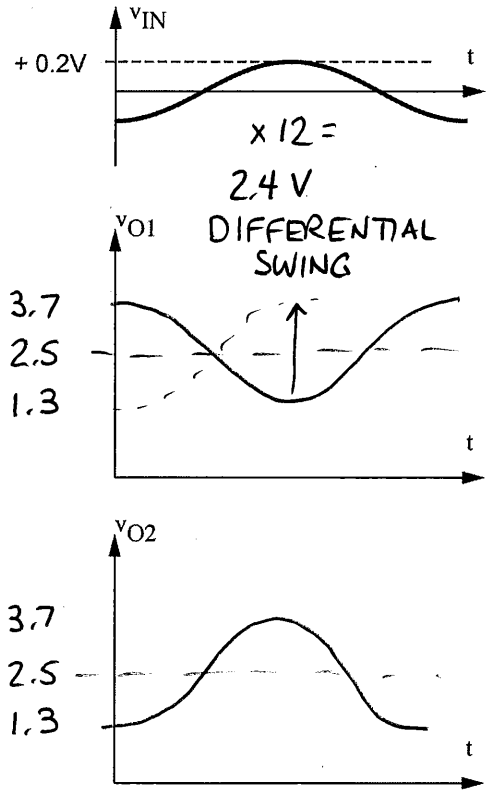
[2]

Explain!: Why or why not?

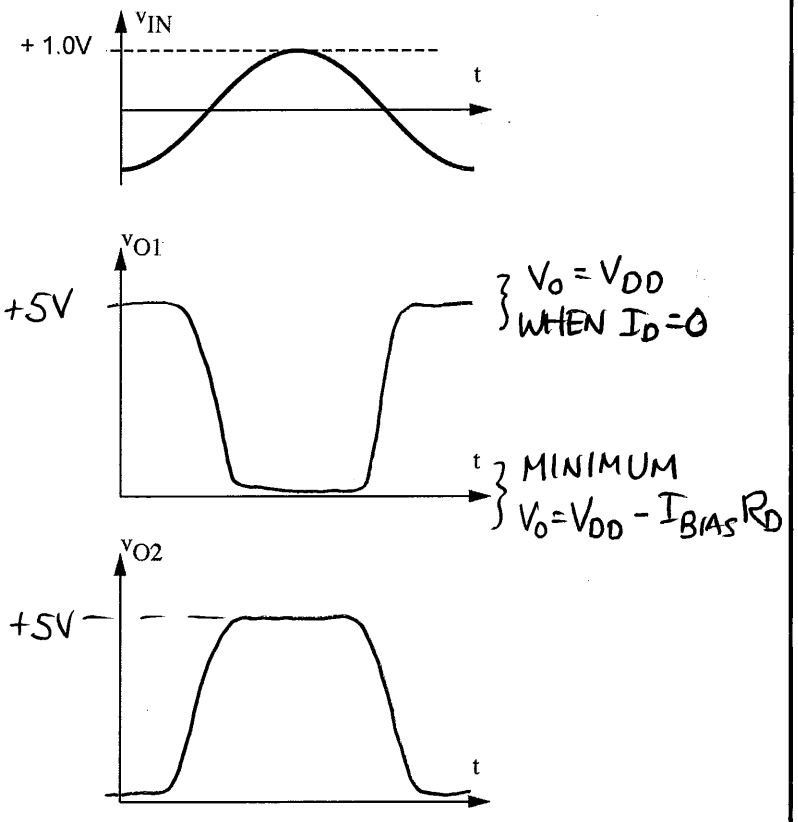
g_m HIGHER (V_{OV} LOWER)



Axes for (d):



Axes for (e):



5. You are designing analog circuitry on a digital IC being fabricated in a CMOS process with very short gate length (L=0.13μm). The I_D vs. V_{GS} plot for a MOSFET in the active region (measured using the circuit shown in Fig. 4a) is shown below. The characteristic exhibits a "short-channel" effect: due to velocity saturation of carriers in the channel, the mobility relationship does not hold and the square law equation does not apply for predicting drain current I_D when $V_{GS} > 0.5V$

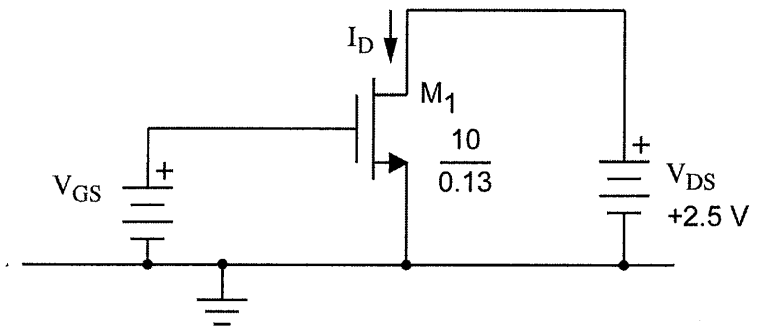
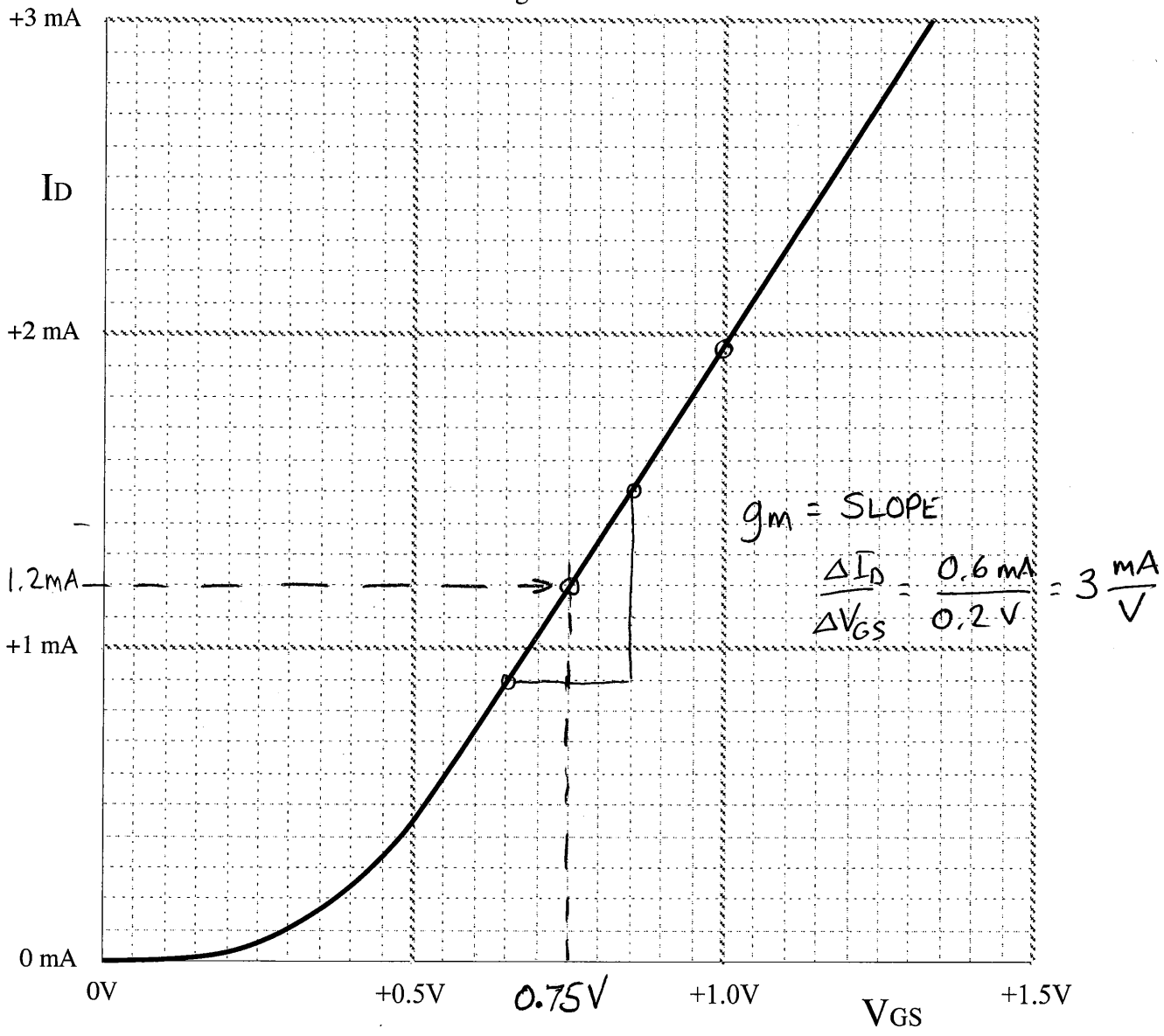
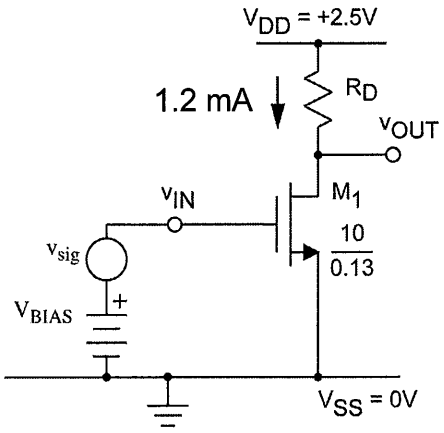


Fig. 4a.



It is desired to use this MOSFET in a common-source amplifier configuration shown below, in which the small-signal input v_{sig} rides on a DC bias level V_{BIAS} which is chosen for a DC drain current of 1.2mA.



a) Find the required DC bias level V_{BIAS} to realize the operating point with DC drain current of 1.2mA. Indicate the operating point on the I_D-V_{GS} plot. **[3]**

V_{BIAS} = 0.75 V

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b) Determine the transconductance g_m at this operating point. **[3]**

g_m = 3.0 E-3 SLOPE

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c) Determine the value of R_D for an output DC bias level of +1.0V **[3]**

R_D = 1.25 kΩ OHM'S LAW

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d) Determine the small signal gain $a_v = v_{out}/v_{sig}$ of the circuit with your value of R_D. You may ignore channel length modulation. **[3]**

a_v = -2.09 $-g_m R_D$ SAME SMALL SIGNAL MODEL FOR COMMON SOURCE

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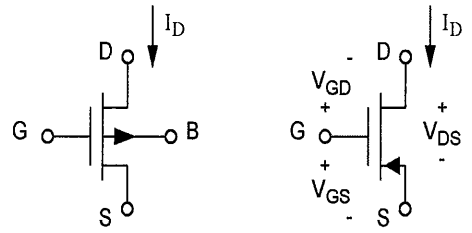
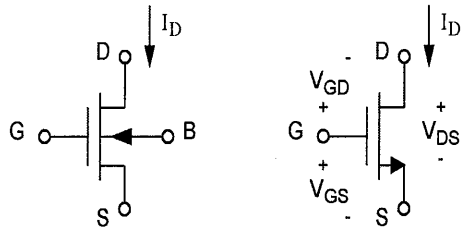
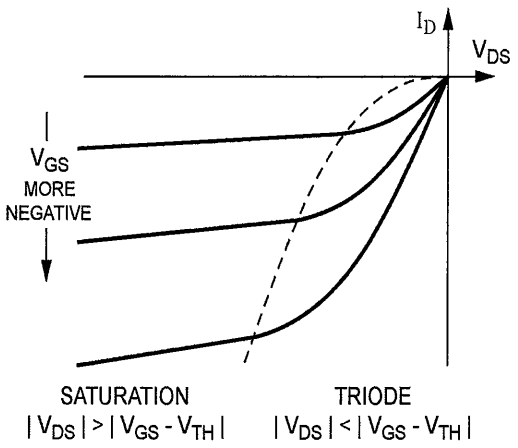
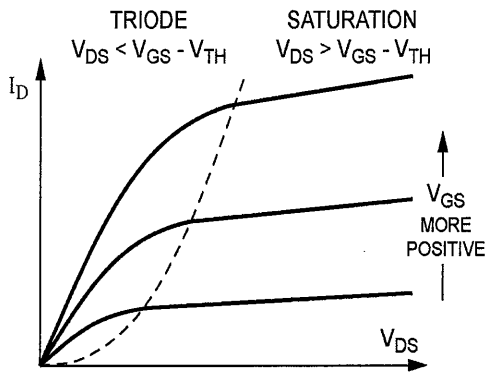
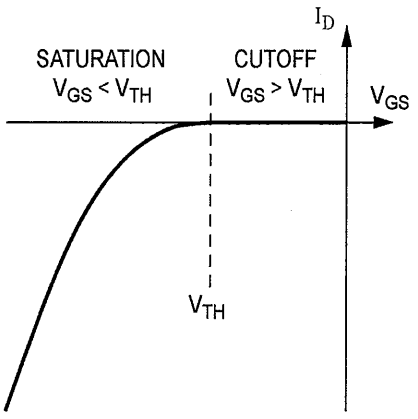
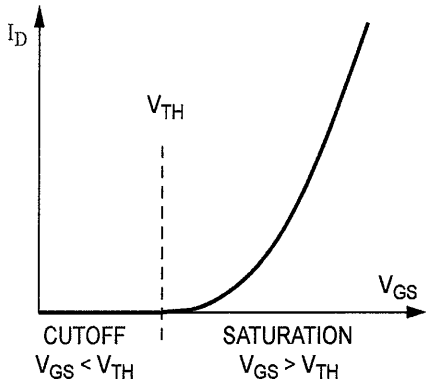
e) A colleague cites the equation $g_m = 2I_D/(V_{GS} - V_{TH})$ and suggests that the small-signal transconductance g_m for this device can be increased, by increasing V_{BIAS} to operate the MOSFET at a higher value of drain current I_D. Is this correct? Explain your answer! **[1]**

YES, g_m WILL BE HIGHER WITH INCREASED I_D

NO, g_m WILL NOT BE HIGHER WITH INCREASED I_D

Explain! SAME SLOPE! g_m DOES NOT CHANGE AT HIGHER V_{GS} VALUES! **[2]**

MOSFET LARGE SIGNAL CHARACTERISTICS

	P CHANNEL	N CHANNEL
CIRCUIT SYMBOL		
SATURATION REGION	$I_D = -\frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2[1 + \lambda\lvert V_{DS}\rvert]$	$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2[1 + \lambda V_{DS}]$
I_D-V_{DS} CHARACTERISTIC		
I_D-V_{GS} CHARACTERISTIC (SATURATION REGION)		
TRIODE REGION	$I_D = -\mu_p C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$	$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$