Name SOLUTIONS

ECE Box # _____

A 90-100
B 75-89
C 60-74

μ 78.3
σ 14.5
MED 80

Problem	Score	Points
1	37.1	40
2	23.4	30
3	17.8	30

ECE4902 B2015

Analog IC Design

Quiz 1

November 6, 2015

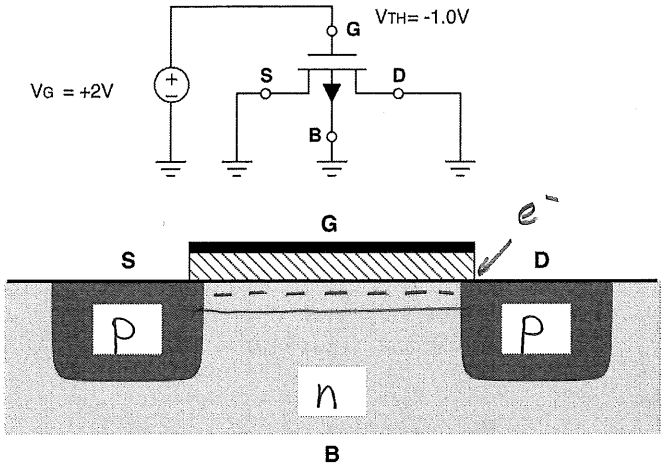
- This is a **closed book, closed notes test**! Use of calculators is OK, but **no pre-stored data or formulas allowed**!
- The last page is a notes page which may be detached for convenience and need not be turned in with the exam
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- **Look for the simple, straightforward way to solve the problem for the level of accuracy required. Don't get entangled in unnecessary algebra.**
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- You have 40 minutes to complete this quiz. There are three problems on a total of 9 pages (including notes page).

1. Parts (a) - (e) give various MOSFET circuit configurations with the given gate voltage V_G with drain and source connected to ground. Also given are the threshold voltage V_{TH}, and cross-sectional views of the MOSFET device. In each case:

i) Indicate whether the MOSFET is an n-channel or p-channel device.
ii) In the boxes in the source, drain, and body regions write "n" or "p" to indicate whether that region is n-type or p-type silicon
iii) Sketch the distribution of <u>mobile</u> charge in the channel (if any), and indicate what kind of charge (holes or e-)
iv) Indicate whether the MOSFET channel is in the accumulation, depletion, or inversion region of operation

a) **[8]**

Circle one: n-CHANNEL (p-CHANNEL)

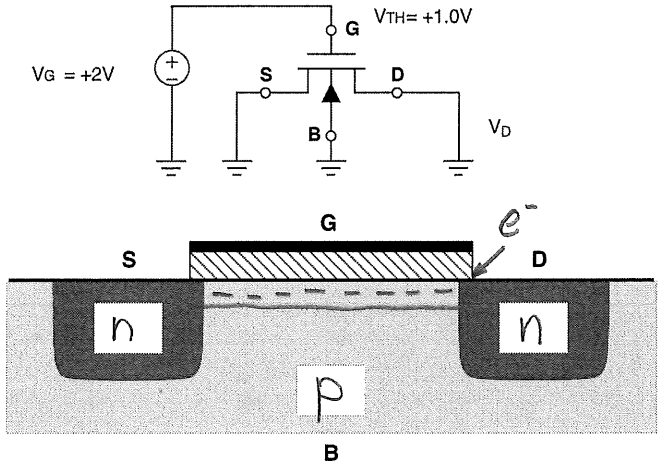


Circle one: (ACCUMULATION) DEPLETION INVERSION

---

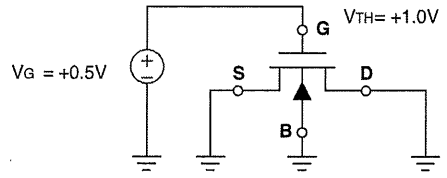
b) **[8]**

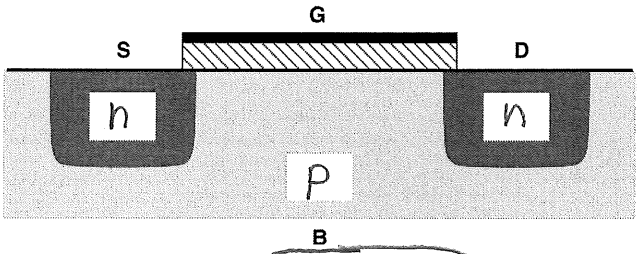
Circle one: (n-CHANNEL) p-CHANNEL



Circle one: ACCUMULATION DEPLETION (INVERSION)

c) Circle one: n-CHANNEL p-CHANNEL **[8]**

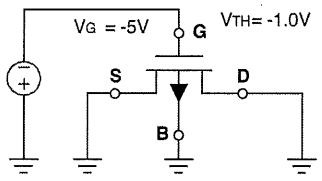


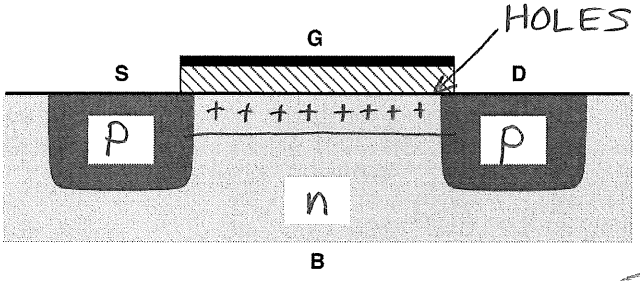


Circle one: ACCUMULATION DEPLETION INVERSION

---

d) Circle one: n-CHANNEL p-CHANNEL **[8]**

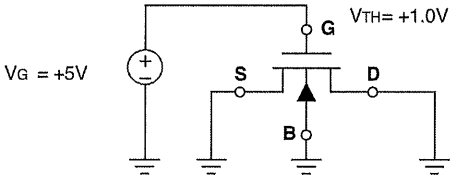


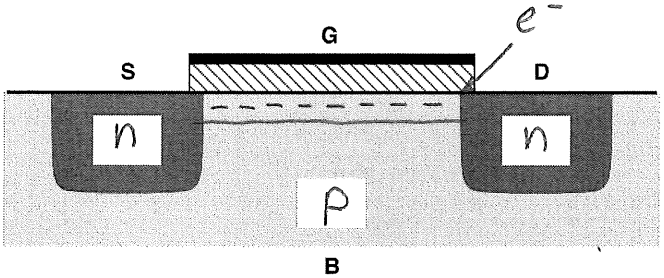


Circle one: ACCUMULATION DEPLETION INVERSION

---

e) Circle one: n-CHANNEL p-CHANNEL **[8]**





Circle one: ACCUMULATION DEPLETION INVERSION

2. On your summer internship as an integrated circuit designer, you are in charge of physical design of the resistors and capacitor for an integrated version of an LM555 oscillator, shown in schematic form on the opposite page. Recalling the circuit from ECE3204, you remember the expressions for the oscillator period

$$T = 0.693(R_A + 2R_B)C$$

and the duty cycle (output "high" time as a fraction of the period) D:

$$D = \frac{2R_B}{R_A + 2R_B}$$

Also shown is a layout view of the resistors and capacitor (top view; onto the surface of the wafer). For the purposes of this problem, you may ignore the effects of contact resistance. The resistor values are equal, $R_A = R_B = 5k\Omega$. For the resistor design, you have a choice of the following layers:

Layer	POLY	NWELL	Units
Sheet resistance	26	1760	Ω / sq

a) Determine the required lengths of the resistor in each material, if width of each is chosen to be $W_{R(POLY)} = W_{R(NWELL)} = 4\mu m$. **[6]**

$L_{R(POLY)} =$ 769 µm

$\frac{5k\Omega}{26\Omega/\square} = 192\square \times 4\mu m$

$L_{R(NWELL)} =$ 11.4 µm

$\frac{5k\Omega}{1.76k\Omega/\square} = 2.84\square \times 4\mu m$

---

b) Which resistor material is the better choice for cost purposes? (Circle one) **[2]**

POLY (NWELL)

Explain!: SMALLER AREA

The capacitor value is to be 30pF (3E-11 F). For the capacitor, you use a poly-poly capacitor with a capacitance per unit area of 1.115E-15 F/μm^2:

Layer	POLY	Units
Poly	1115	aF/um^2

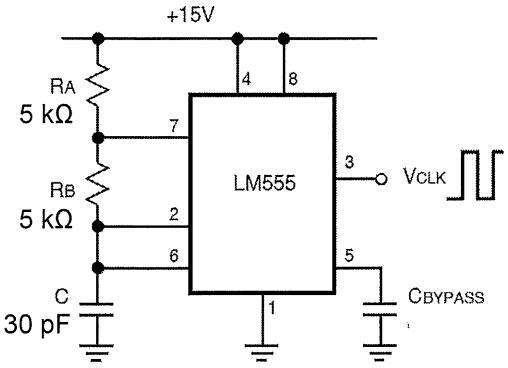
c) Determine the size of the capacitor, if a square shape is chosen with the length and width equal as shown. **[6]**

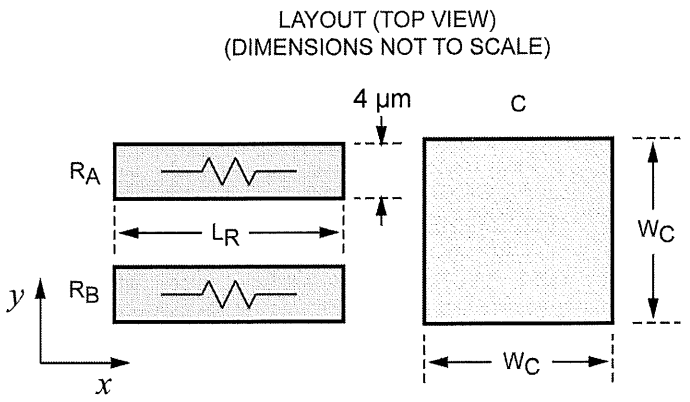
$W_C =$ 162 µm

$3E\text{-}11\ F = \left(1.115E\text{-}15\ \frac{F}{\mu m^2}\right) W_C^2$

$\Rightarrow W_C = \sqrt{\frac{3E\text{-}11}{1.115E\text{-}15}}$

Parts (d-g) are concerned with variation in component values caused by variations in the manufacturing process.



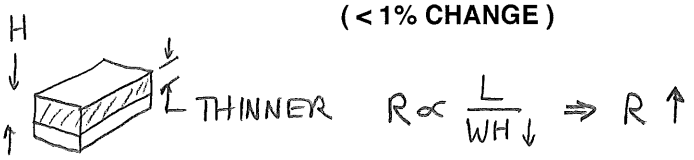


In one production run, the wafers are removed from a deposition step too soon and the thickness (z dimension) of the resistor material you chose in (b) is 20% less than normal.

d) Period: With the thinner-than-normal layer, will the actual value of the oscillator <u>period</u> be lower, unchanged, or higher? Circle one and explain: **[1]**

LOWER **ABOUT THE SAME (< 1% CHANGE)** **HIGHER**

Explain!: **[3]**



e) Duty Cycle: With the thinner-than-normal layer, will the actual value of the oscillator <u>duty cycle</u> be lower, unchanged, or higher? Circle one and explain: **[1]**

LOWER **ABOUT THE SAME (< 1% CHANGE)** **HIGHER**

[3]

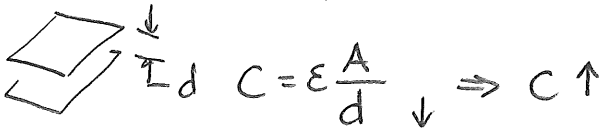
Explain!: BOTH R CHANGE THE SAME WAY
⇒ RATIO UNCHANGED

In a different production run, the resistors are OK but the wafers are removed from an oxide growth step too soon and the thickness (z dimension) of the insulating material between the polysilicon layers in the poly-poly capacitor is 20% less than normal.

f) Period: With the thinner-than-normal layer, will the actual value of the oscillator <u>period</u> be lower, unchanged, or higher? Circle one and explain: **[1]**

LOWER **ABOUT THE SAME (< 1% CHANGE)** **HIGHER**

Explain!: **[3]**



g) Duty Cycle: With the thinner-than-normal layer, will the actual value of the oscillator <u>duty cycle</u> be lower, unchanged, or higher? Circle one and explain: **[1]**

LOWER **ABOUT THE SAME (< 1% CHANGE)** **HIGHER**

Explain!: **[3]**

C NOT INVOLVED IN DUTY CYCLE EXPRESSION

3. On your first job as an IC designer, you are working on the physical design of resistors R1 and R2 in the circuit shown on the opposite page. Also shown is a layout view of the resistor dimensions (top view; onto the surface of the wafer).

The input v_{in} is a 2.83 V peak (2V rms) sine wave. The purpose of the circuit is to provide a precisely attenuated version of v_{in} at v_{out}. The low value (150Ω) of resistors is necessary to maintain a 75Ω output resistance at the v_{out} node for analog video impedance matching.

The resistors will be implemented in a POLY layer with parameters as shown on the opposite page.

The minimum of either dimension (L or W) is 4μm. Note that, depending on the requirements on the design, it may be necessary for both L and W to be greater than 4μm. For the purposes of this problem you may ignore the area needed for contacts, as well as contact resistance.

Looking back on your ECE4902 experience, you recall that your professor never went into much detail on all the possible factors influencing resistor design. So your on-the-job training is an example of the lifelong learning that WPI has prepared you for.

---

a) You do remember that minimizing area is an important economic consideration. Determine the length L_R and width W_R for the resistor that will realize the value of 150Ω with minimum area. Numerical values required; accuracy ±10%. **[10]**

L_R = 23μm W_R = 4μm } USE MINIMUM

$\frac{150\,\Omega}{26\Omega/\square} = 5.76\,\square \times 4\mu m$

---

b) A colleague points out that a larger area will improve matching, but not to make the resistors too large due to the parasitic capacitance to the substrate. Determine the length L_R and width W_R for the resistor that will realize the value of 150Ω with a parasitic capacitance (for each resistor) of 100fF. Numerical value required; accuracy ±10%. **[10]**

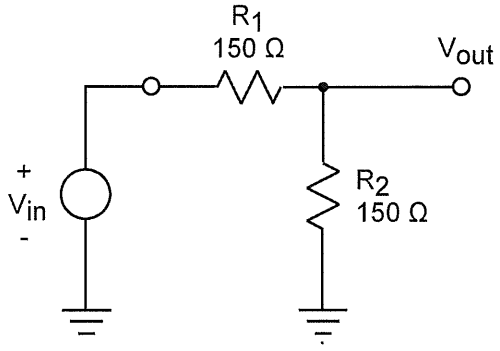
L_R = 62μm W_R = 10.8μm

---

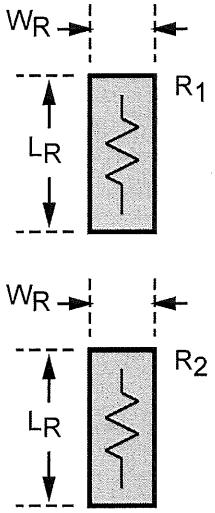
c) Another colleague insists that a 100fF capacitance won't be an issue, but power dissipation may be a problem. If the power dissipation exceeds a density of 1$\mu W/\mu m^2$, the silicon die may overheat. Determine the length L_R and width W_R for the resistor that will realize the value of 150Ω with power density (for each resistor) of 1$\mu W/\mu m^2$. Numerical value required; accuracy ±10%. **[10]**

L_R = 196μm W_R = 34μm

Parameter	Value	Units
Sheet resistance	26	Ω / sq
Capacitance to substrate	0.15	fF/μm^2



R1, R2 LAYOUT (TOP VIEW)
(DIMENSIONS NOT TO SCALE)



b) FOR C_{par} = 100fF, AREA WILL BE

$100fF = L\,W\ 0.15\ fF/\mu m^2$

$\Rightarrow LW = \frac{100fF}{0.15fF/\mu m^2} = 667\,\mu m^2$

FOR VALUE, STILL NEED RATIO $L = 5.76\,W$

$\underbrace{(5.76\,W)}_{L}\,W = 667\,\mu m^2 \Rightarrow W = \sqrt{\frac{667\,\mu m^2}{5.76}} = 10.8\,\mu m$

$L = 5.76\,W = 62\,\mu m$

---

c) POWER DISSIPATED: 1 V rms ON EACH

$P = \frac{1V^2}{150\Omega} = 6.67\ mW$

NEED AREA (FOR $1\mu W/\mu m^2$) OF $\frac{6.67\,mW}{1\mu W/\mu m^2} = 6670\,\mu m^2$

SIMILAR TO (b)

$5.76\,W^2 = 6670\,\mu m^2 \Rightarrow W = 34\,\mu m \quad L = 196\,\mu m$