A	91 - 100
B	80 - 90
C	65 - 79

M	88.2
σ	11.7
MED	90

Name SOLUTIONS

ECE Box # _____

Problem	Score	Points
1	28.5	30
2	37.9	40
3	21.8	30

ECE4902 B2015

Analog IC Design

Quiz 2

November 13, 2015

- This is a **closed book, closed notes test!** Use of calculators is OK, but **no pre-stored data or formulas allowed!**
- The last page is a notes page which may be detached for convenience and need not be turned in with the exam
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- **Look for the simple, straightforward way to solve the problem for the level of accuracy required. Don't get entangled in unnecessary algebra.**
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- You have 40 minutes to complete this quiz. There are three problems on a total of 13 pages (including notes page).

1. Parts (a) - (c) give various MOSFET circuit configurations with the given V_{GS}, V_{DS}, and threshold voltage V_{TH}, and cross-sectional views of the MOSFET device. In each case:

i) Indicate whether the MOSFET is an n-channel or p-channel device.

ii) In the boxes in the source, drain, and body regions write "n" or "p" to indicate whether that region is n-type or p-type silicon

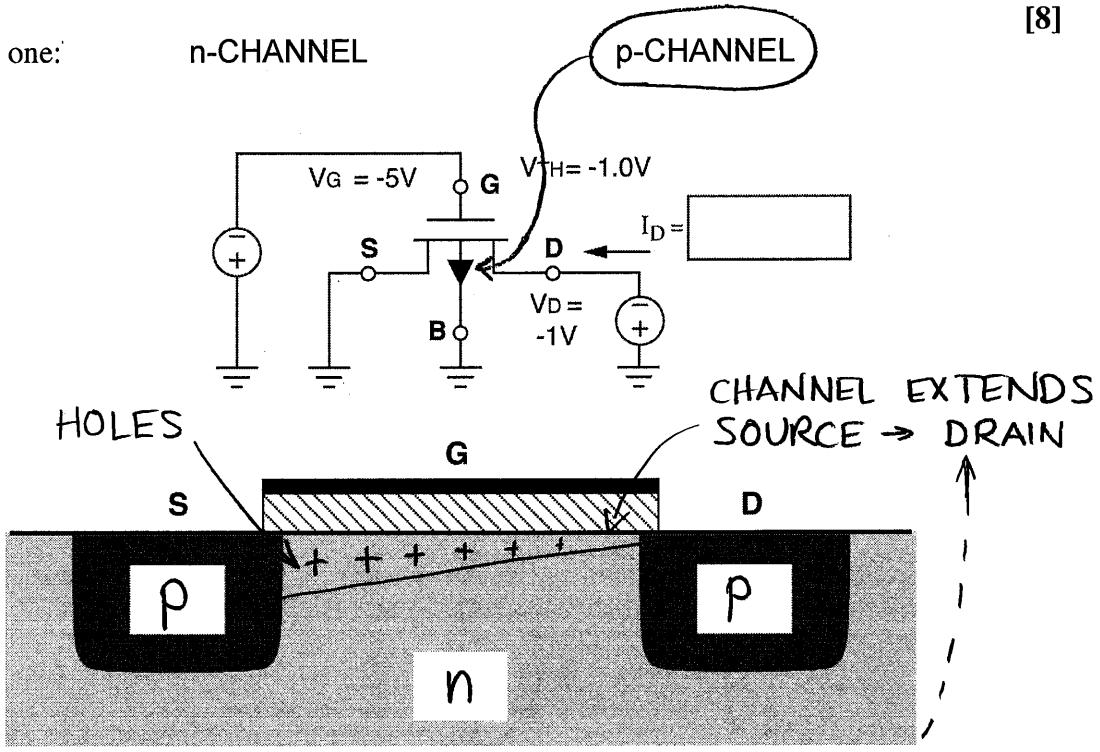
iii) Sketch the distribution of mobile charge in the channel (if any), and indicate what kind of charge (holes or e-). IF THE DISTRIBUTION OF MOBILE CHARGE SHOULD BE NONUNIFORM ALONG THE LENGTH OF THE CHANNEL, BE SURE YOUR PLOT SHOWS THIS!!

iv) Indicate whether the MOSFET is in the cutoff, triode, or saturation region of operation

v) Choose ONLY ONE of (a) - (c), indicate the drain current I_D in the box provided. **[6]**
Your choice!

a) **[8]**

Circle one: n-CHANNEL p-CHANNEL

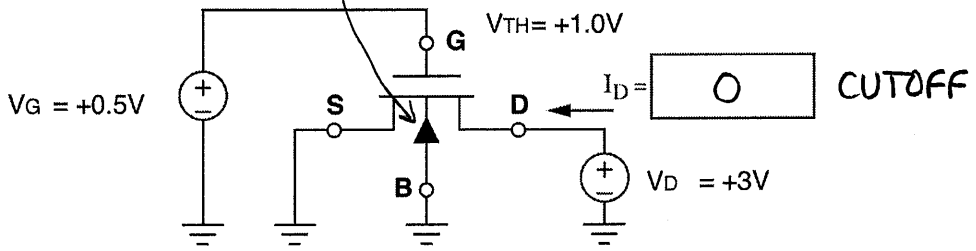


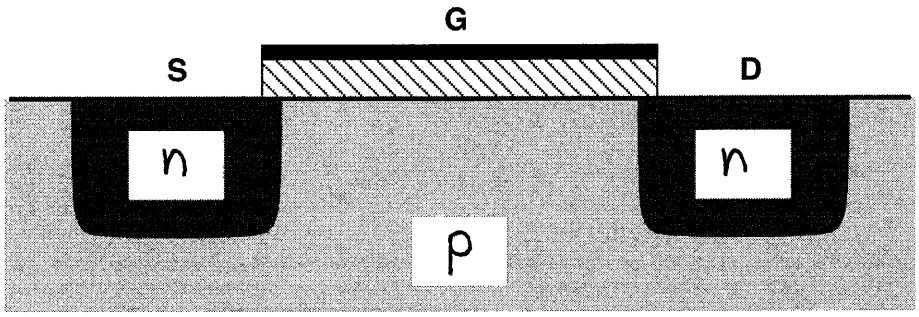
Circle one: ~~CUTOFF~~ TRIODE ~~SATURATION~~

$V_{GS} < V_{TH}$ $|V_{GS} - V_{TH}| > |V_{DS}|$

b) [8]

Circle one: n-CHANNEL p-CHANNEL





$V_{GS} < V_{TH}$

Circle one: CUTOFF TRIODE SATURATION

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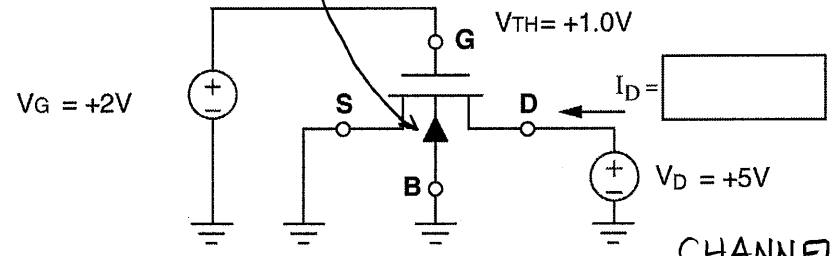
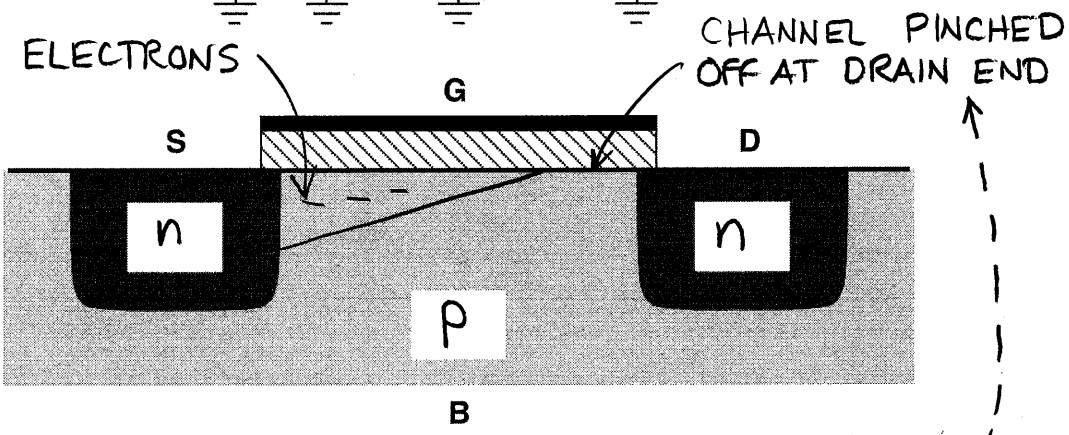
c) [8]

Circle one: n-CHANNEL p-CHANNEL





Circle one: ~~CUTOFF~~ ~~TRIODE~~ SATURATION

$V_{GS} > V_{TH}$ $V_{GS} - V_{TH} < V_{DS}$

2. Even Digital is Analog: LVDS

Low Voltage Differential Signaling (LVDS) is a standard for transmitting logic signals in differential form. For high speed data (>100s of Mb/s) it has several advantages over single-ended logic signal transmission, which given the time constraints of a quiz we won't consider now.

A functional diagram of the LVDS concept is shown in the figure on the opposite page.

To send a logic "high" as shown in the figure, MOSFETs M1 and M2 are turned on and M3 and M4 are off. The current from the 3.5mA current source flows through the 100Ω resistor, giving a +350mV drop, plus-to-minus, as shown at the receiver.

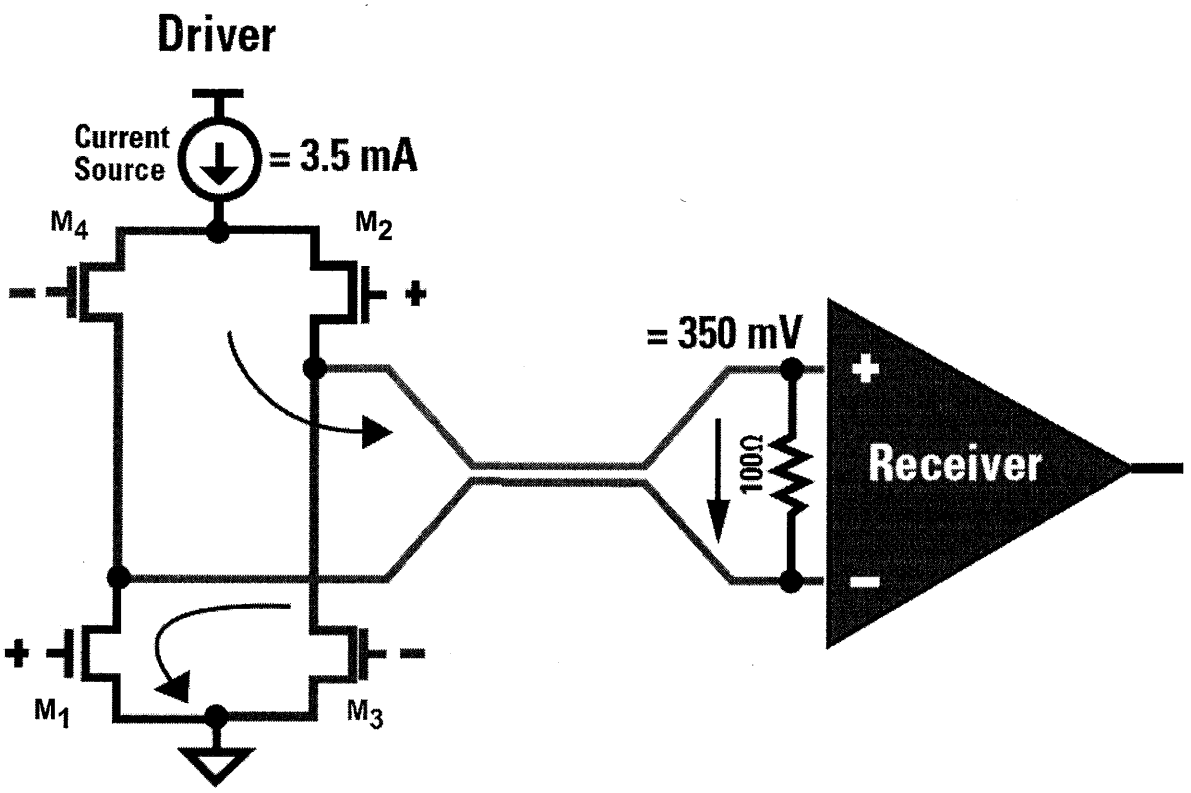
To send a logic "low" M3 and M4 are turned on; M1 and M2 are turned off. The direction of current flow in the 100Ω load is reversed, giving a -350mV drop at the receiver.

Important considerations in the design of the driver are:

i) Minimizing the voltage drops on the M1-M4 switches when "on." In the case shown in the figure, any voltage drop across M1 and M2 will add in series with the 350mV, reducing the headroom available for the 3.5mA current source.

ii) Ensuring the 3.5mA current source will function properly, given the voltage drops across M1, M2, and the 100Ω load resistance.

We'll look at these considerations separately in parts (a-b) and (c-e) of this problem. Note that these parts do not depend on each other, so if you get stuck on (a-b) you can try (c-e), or vice versa.



Source: http://www.ti.com/lit/ml/snla187/snla187.pdf

First, we'll size the width W5 of MOSFET M5 in the current source. The circuit configuration is shown in the figure on the opposite page. Note that M5 is a PMOS device.

The length is set at L5=2μm. The source of M5 is connected to the +3.3V supply voltage and the gate is connected to ground. Our goal is a drain current of 3.5mA. Assume the drain voltage of M5 will be +0.45V (we will ensure this by design in parts (c-e).

For the MOSFET parameters, use the following:

Parameter	N-channel	P-channel	Units
V_{TH}	+0.65	-0.80	V
μC_{ox}	2.5E-4	7.0E-5	A/V^2

a) What is the operating region (cutoff, triode, saturation) for M5 in this condition?

Circle one: ~~CUTOFF~~ ~~TRIODE~~ (SATURATION) **[8]**

$V_{GS} < V_{TH}$ $|V_{DS}| > |V_{GS} - V_{TH}|$

2.85V 2.5V

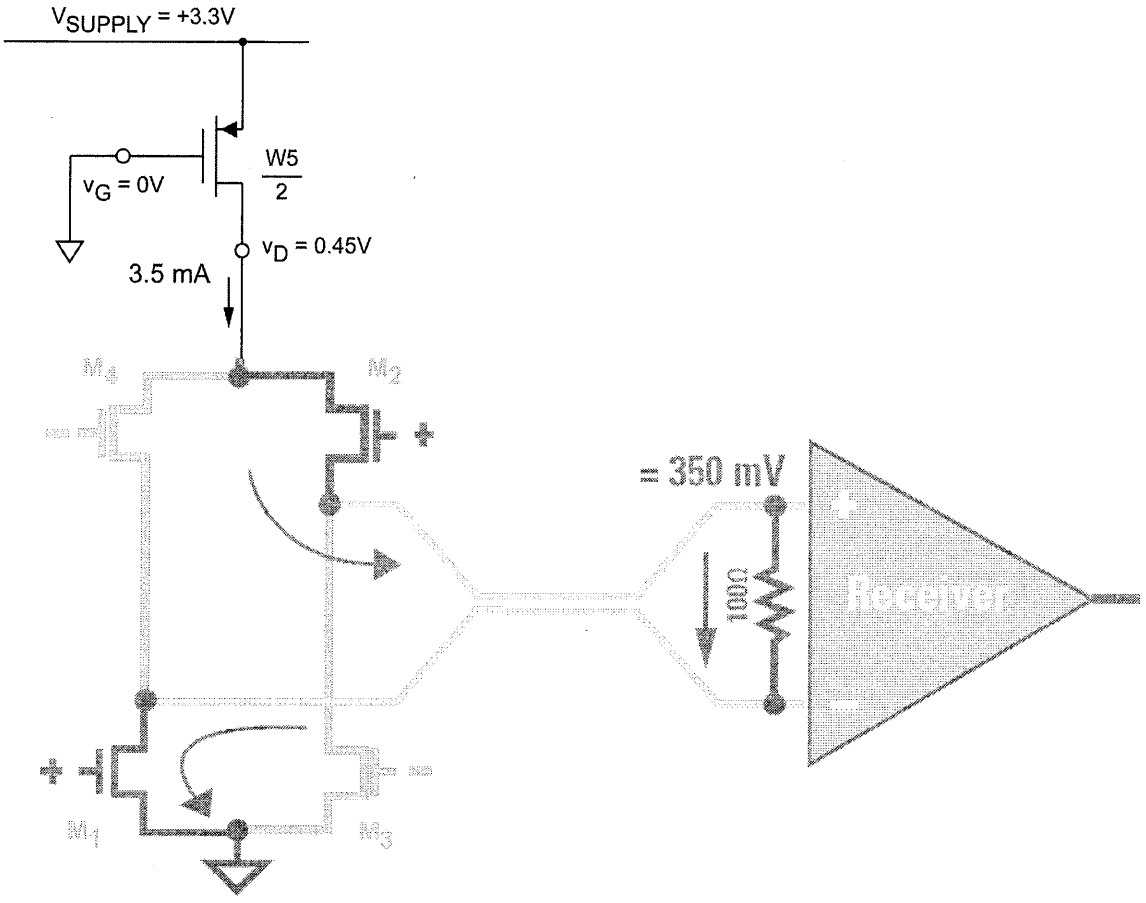
---

b) Determine the width W5 necessary to meet the requirement of a 3.5mA drain current in this condition. **[8]**

W5 = 32μm

SQUARE LAW: $3.5\,mA = \frac{7E\text{-}5}{2}\frac{W_5}{2\mu m}(-3.3V-(-0.8V))^2$

$\Rightarrow W_5 = \frac{4(3.5\,mA)}{(7E\text{-}5)(2.5V)^2} = 32\mu m$


V_{SUPPLY} = +3.3V
v_G = 0V
W5
2
v_D = 0.45V
3.5 mA
M_4
M_2
= 350 mV
100Ω
Receiver
M_1
M_3

Next, we'll size the width W1 of MOSFET M1. The circuit configuration is shown in the figure on the opposite page.

The length is set to the minimum, L1=0.5µm in this process. M1 is turned "on" by applying +3.3V at the gate. Our goal is a 50mV voltage drop from drain to source when the drain current is 3.5mA.

For the MOSFET parameters, use the following:

Parameter	N-channel	P-channel	Units
V_{TH}	+0.65	-0.80	V
μC_{ox}	2.5E-4	7.0E-5	A/V^2

c) What is the operating region (cutoff, triode, saturation) for M1 in this condition?

Circle one: ~~CUTOFF~~ (TRIODE) ~~SATURATION~~ **[8]**

$V_{GS} > V_{TH}$

$V_{DS} < V_{GS} - V_{TH}$

0,05V 2,65V

---

d) What is the required "on" resistance R_{on} looking into the drain of M1? **[8]**

R_{on} = 14.3Ω $\quad \frac{V_{DS}}{I_D} = \frac{50mV}{3.5mA}$

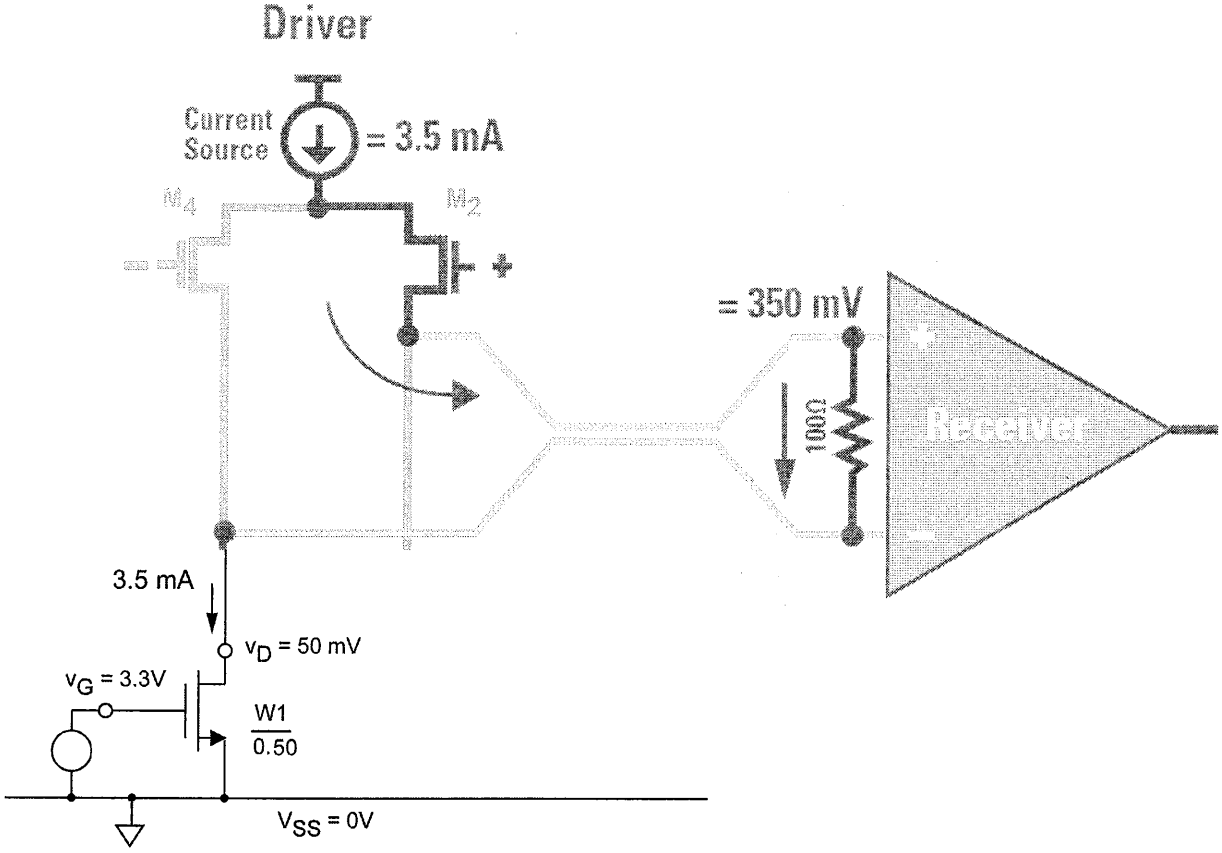
---

e) Determine the width W1 necessary to meet the requirement a 50mV voltage drop from drain to source when the drain current is 3.5mA in this condition. **[8]**

W1 = 52.8µm

R_{on} EQUATION $\quad 14.3\Omega = \frac{1}{(2.5E-4)\frac{W_1}{0.5}(3.3-0.65)}$

$W_1 = 52.8\mu m$



FULL TRIODE EQUATION FOR (e)

$$3.5\,mA = (2.5E\text{-}4)\frac{W_1}{0.5}\left[(3.3-0.65)(0.05)-\frac{(0.05)^2}{2}\right]$$

$W_1 = 53.9\,\mu m$

CLOSE TO RESULT FROM R_{on} APPROXIMATION

3. I'm sure you remember the HW Set 2 "Even digital is analog" logic inverter problem - and in case you don't, the schematic is shown in Figure 3-1 at the top of the opposite page. In that problem you chose a value for R_D so that a 2.5 V "logic middle" at the input would give a 2.5V output when the NMOS device was one of the MOSFETs on the CD4007 array you are using from your ECE lab kit.

In this problem, you are designing a similar circuit in a 0.5 μm CMOS process, shown in Figure 3-2 on the opposite page. Recalling the large value of R_D from the problem set, you decide to implement R_D as MOSFET M2 in triode to save area. You also save area by choosing both devices to have minimum length L1 = L2 = 0.5μm.

For the MOSFET parameters, use the following:

Parameter	N-channel	P-channel	Units
V_{TH}	+0.65	-0.80	V
μC_{ox}	2.5E-4	7.0E-5	A/V^2

For the purposes of this problem you may ignore channel length modulation.

a) In choosing device widths W1 and W2, there are two requirements you must meet given the input condition V_{IN} = +2.5V:

i) For input voltage V_{IN} = +2.5V, the output voltage must be V_{OUT} = +2.5V.

ii) With V_{IN} = +2.5V and V_{OUT} = +2.5V, the drain current I_D = 3mA

Determine W1 and W2 (in μm) to meet conditions (i) and (ii)

[20]

W1 = 3.5μm W2 = 2.0μm - 2.9μm

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b) Assuming M2 acts as a resistor, determine the small-signal gain v_{out}/v_{in} (slope of the v_{IN} - v_{OUT} plot) at the operating point V_{IN} = +2.5V, V_{OUT} = +2.5V.

[10]

v_{out}/v_{in} = -2.7

$$-g_m R_3 = -\underbrace{\frac{2(3mA)}{(2.5-0.65)}}_{g_m = 3.24E\text{-}3\ \frac{A}{V}}(833\Omega) = -2.7$$

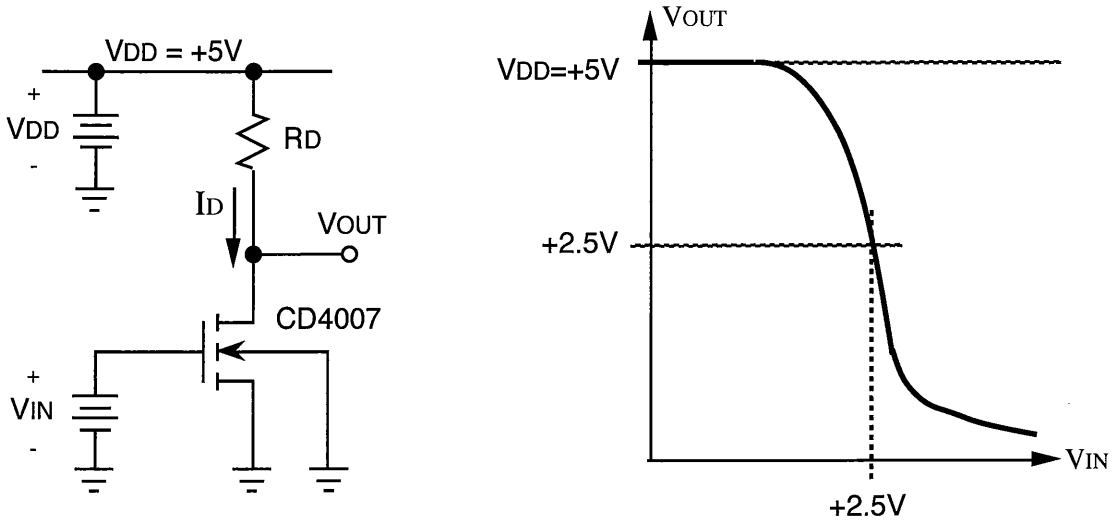
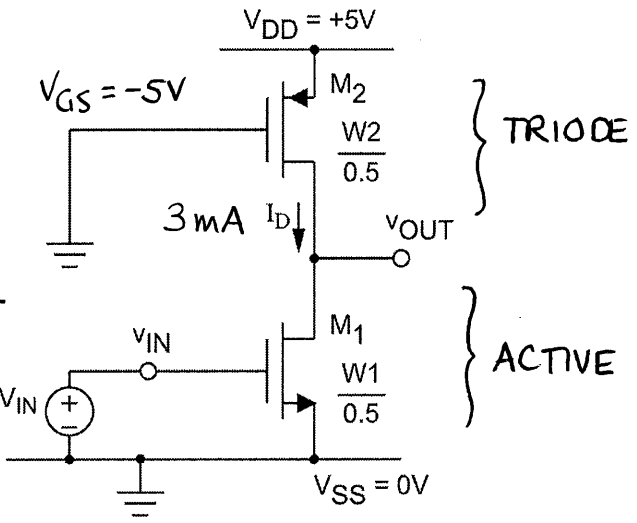


Figure 3-1. Resistive load logic inverter from HW set 2 (not to scale).



M_1:

$3mA = \frac{2.5E\text{-}4}{2}\frac{W_1}{0.5}(2.5V - 0.65V)^2$

$\Rightarrow W_1 = 3.5\,\mu m$

Figure 3-2. Resistive load logic inverter in 0.5 μm CMOS process.
M2 (PMOS in triode) functions as resistive load R_D.

M_2: R_{on} APPROXIMATION

$R_{on} = \frac{2.5V}{3mA} = 833\Omega$

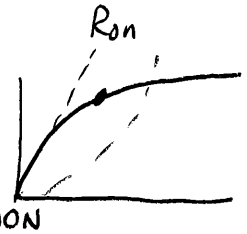
$= \frac{1}{7E\text{-}5\frac{W_2}{0.5}(5V - 0.8V)}$

$W_2 = 2.0\,\mu m$

FULL TRIODE

$3mA = 7E\text{-}5\frac{W_2}{0.5}\left[(5-0.8)(2.5V) - \frac{(2.5V)^2}{2}\right]$

$W_2 = 2.9$



LARGE V_{DS};
R_{on} APPROXIMATION
NOT AS CLOSE