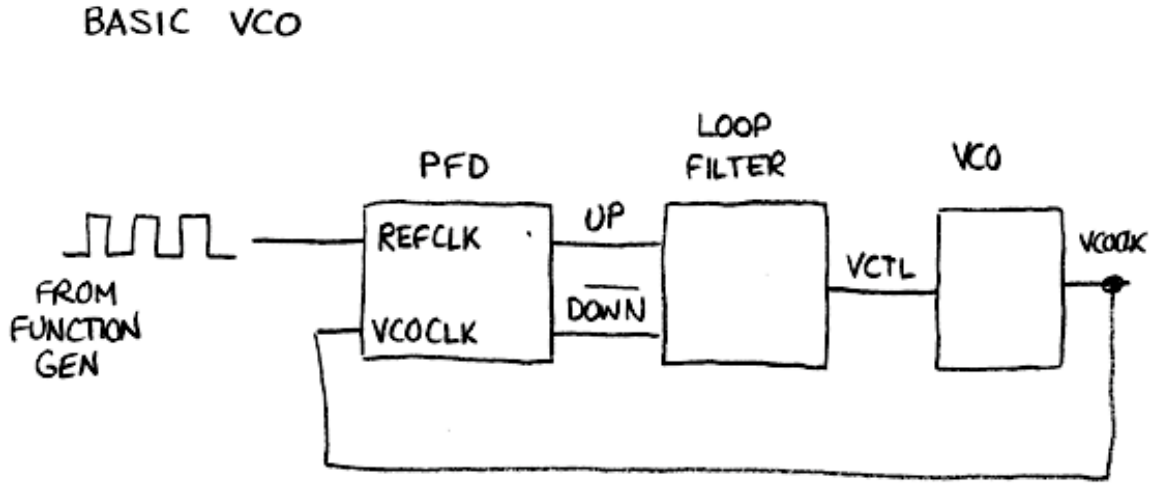
PLL

This is the most complicated of the three optional labs - but is definitely the coolest system and if you can get it working, you should be able to learn a lot.

The top level block diagram of the PLL is shown below:



The system blocks and their input and output signals are as follows:

SYSTEM

INPUT	REFCLK	Reference clock	0 to +5V clock signal
OUTPUT	VCOCLK	VCO clock	0 to +5V clock signal

For the basic VCO, the purpose is to produce an output clock signal VCOCLK that is the same frequency and phase as the input.

PHASE-FREQUENCY DETECTOR (PFD)

INPUT	REFCLK	Reference clock	0 to +5V clock signal
	VCOCLK	VCO clock	0 to +5V clock signal
OUTPUT	UP	VCO freq UP	0 to +5V signal, active high
	/DOWN	VCO freq DOWN	0 to +5V signal, active low

The phase-frequency detector compares the incoming rising edges of the reference clock and VCO clock. If the reference clock edge arrives first, an UP pulse is sent to the loop filter indicating that the VCO needs to speed up to bring the VCO clock into lock with the reference clock. If the VCO clock edge arrives first, then the VCO is running too fast and a /DOWN pulse is sent to the loop filter indicating that the VCO needs to slow down to bring the VCO clock into lock with the reference clock. When the two clocks are locked in phase and frequency then the UP and /DOWN signals are very narrow pulses of equal duration that essentially cancel each other out, leaving the VCO frequency unchanged.

LOOP FILTER

INPUT	UP	VCO freq UP	0 to +5V signal, active high
	/DOWN	VCO freq DOWN	0 to +5V signal, active low
OUTPUT	VCTL	VCO control voltage	Analog signal

The loop filter is essentially a lowpass filter (actually an integrator) that smooths out the pulses from the PFD to provide a smooth control voltage for the voltage controlled oscillator (VCO). Since the entire PLL is a negative feedback loop, it turns out there are some interesting controls problems involved in making sure the system is stable. One of the constraints in loop filter design parameters (e.g. the time constant of the integrator) is ensuring stability.

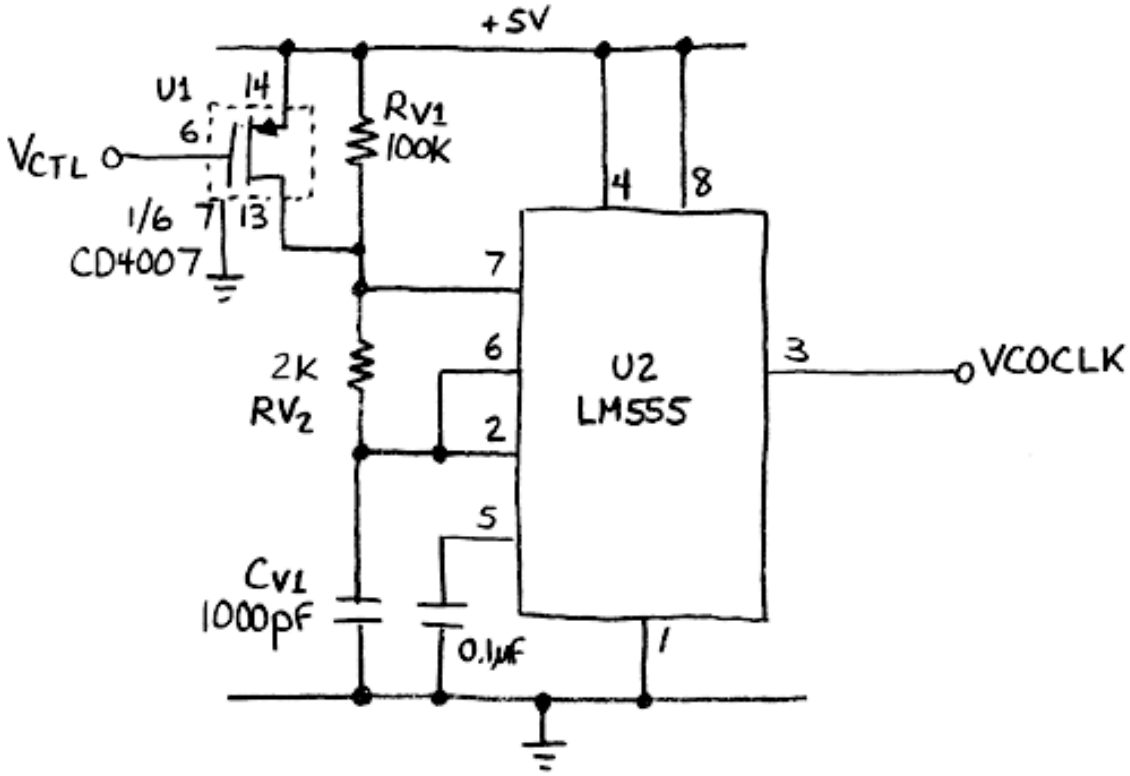
VOLTAGE CONTROLLED OSCILLATOR (VCO)

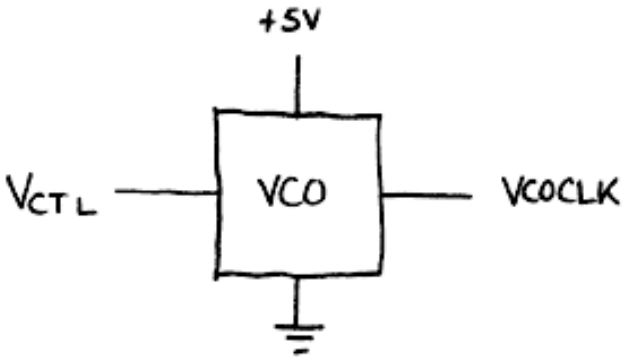
INPUT	VCTL	VCO control voltage	Analog signal
OUTPUT	VCOCLK	VCO clock	0 to +5V clock signal

The VCO provides an output clock with frequency controlled by the level of the (analog) input control voltage. For some VCOs, the output clock needs to be 50% duty cycle; that's not important in this lab which is a good thing since the simple LM555-based VCO we use does not give a 50% duty cycle output.

BULDING THE SYSTEM

The first step is to build the VCO block by itself and verify its operation:



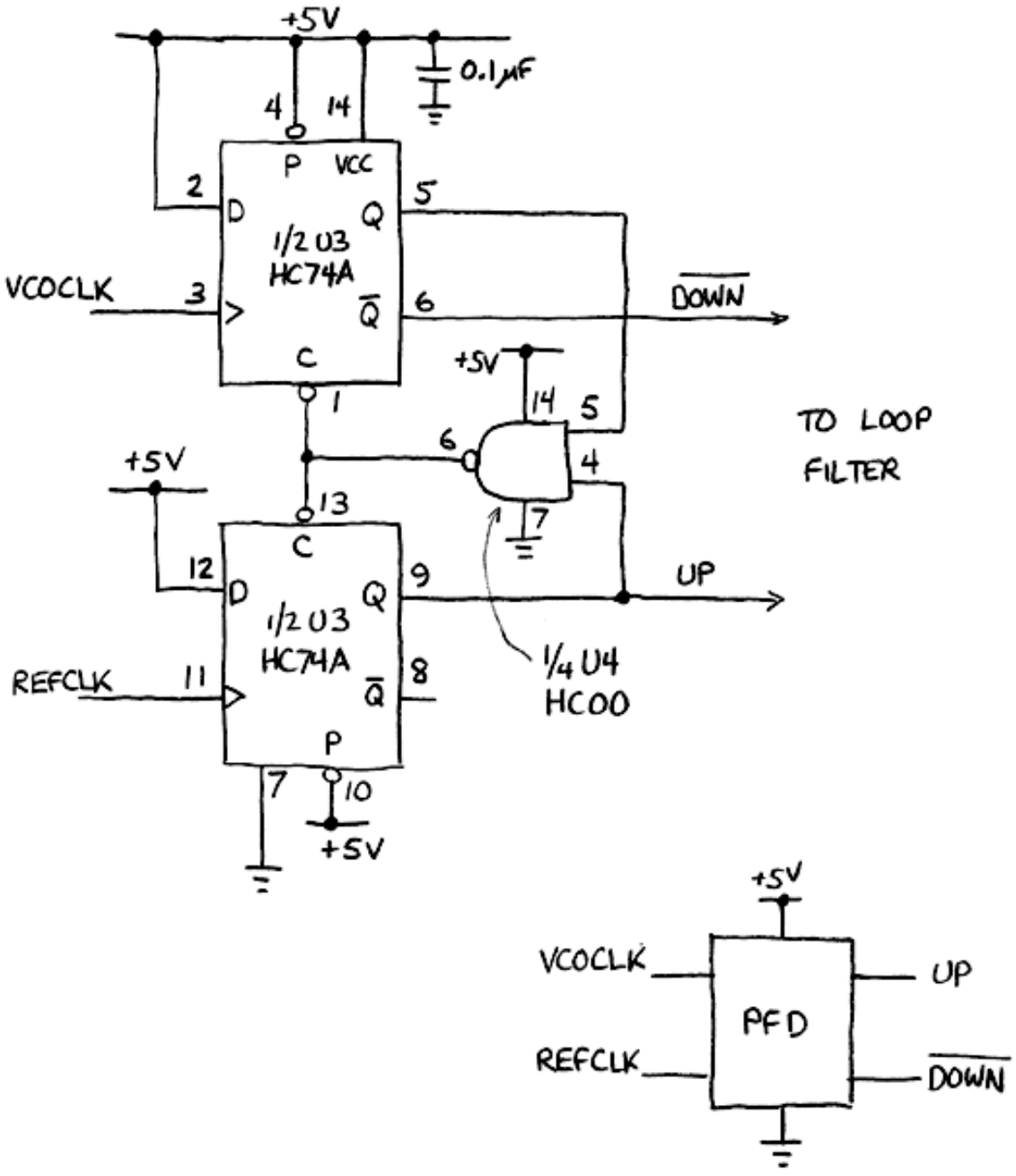


R_{V1} and R_{V2} are the resistors normally used in the LM555 clock circuit. The voltage control of frequency is achieved by using a MOSFET in triode as a voltage controlled resistor in parallel with RV1.

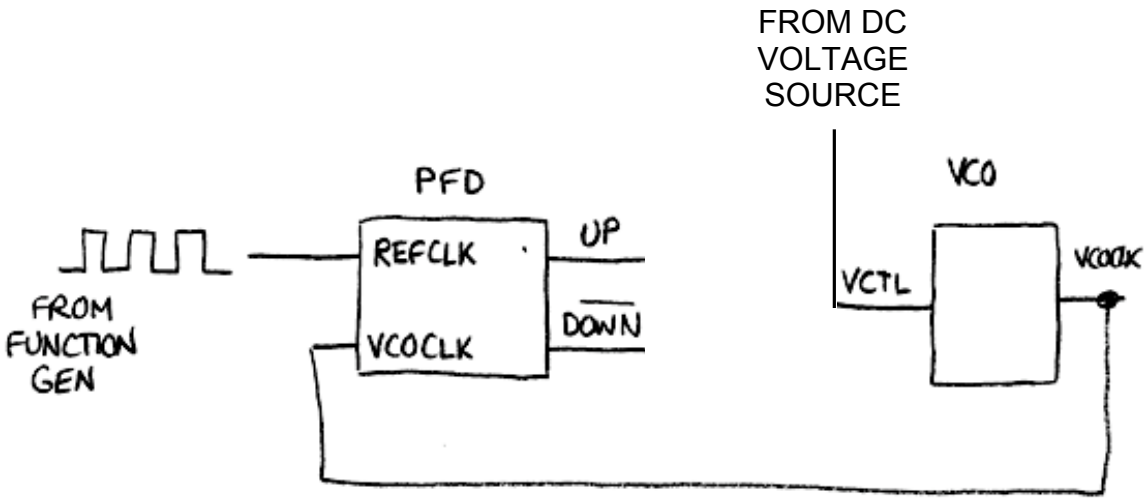
Test the operation of your VCO by using a DC voltage source for V_{CTL} (one of the adjustable power supply outputs). Apply a range of values (about 10-15 data points) for V_{CTL} (from 0V to 5V), and measure the output frequency in each case. Plot the output frequency as a function of V_{CTL}. Be sure to note the range of frequencies the VCO is capable of producing!

NEXT: THE PFD

Next build the PFD:



Wire up the VCO output to the VCOCLK input of the PFD, and apply a 0 to +5V clock from the function generator to REFCLK (See next page).



With this setup, you are able to independently control the frequencies of REFCLK and VCOCLK, and therefore test the operation of the phase-frequency detector. Adjust the function generator and VCO clock frequencies relative to each other to verify the following:

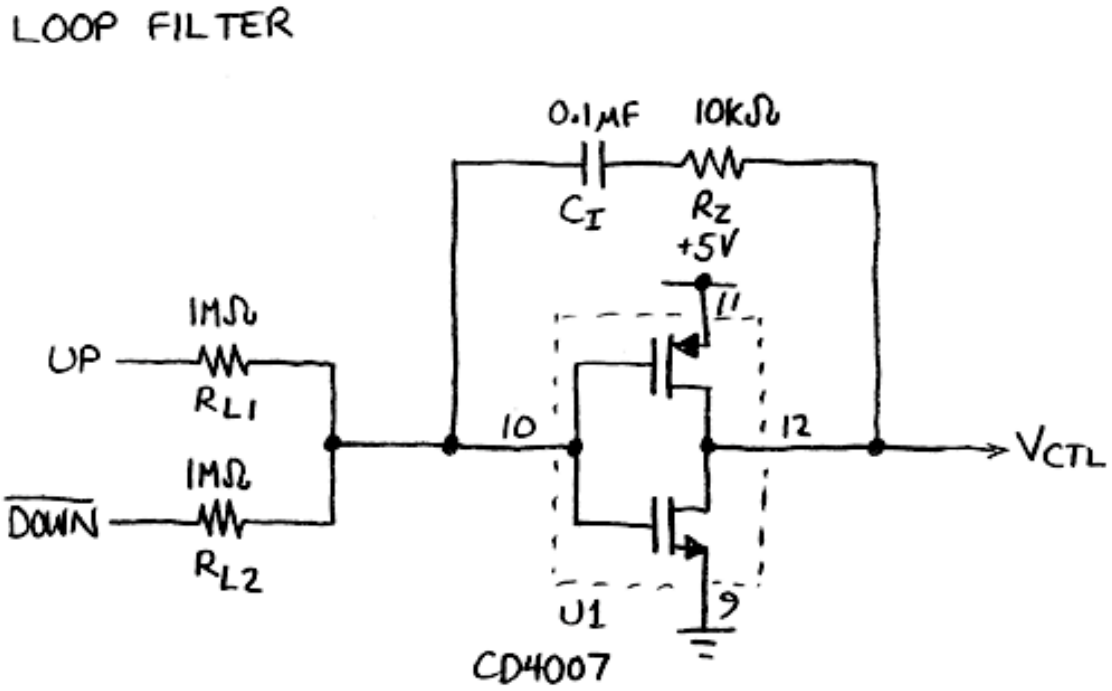
With the REFCLK frequency greater than the VCO frequency, you should see high pulses on the UP output of the PFD, and the /DOWN signal should be mostly inactive (high).

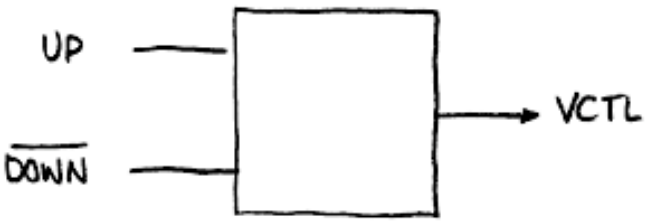
With the VCO frequency greater than the REFCLK frequency, you should see low pulses on the /DOWN output of the PFD, and the UP signal should be mostly inactive (low).

Once you've verified the PFD operation, it's time to build the loop filter and close the loop!

FINALLY: THE LOOP FILTER

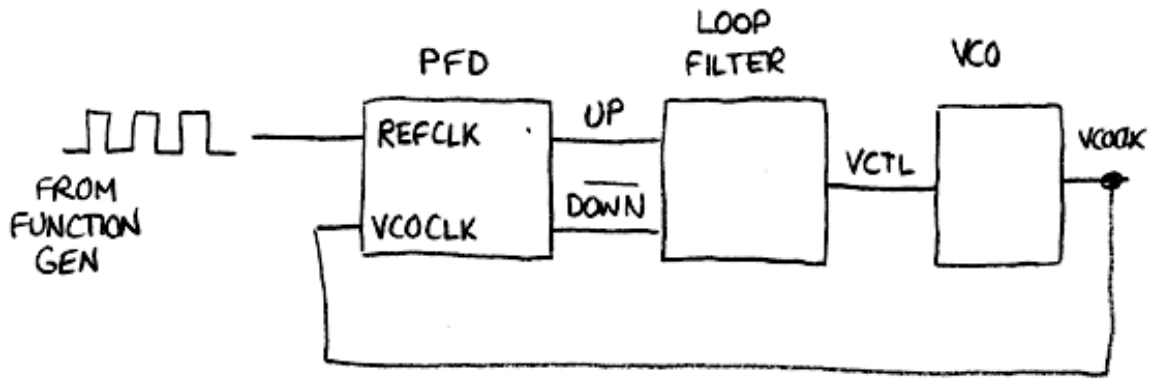
Build the loop filter:





which cheesily uses the MOSFETs of the CD4007 in a CMOS inverter configuration as an inverting op-amp with open-loop gain of around 30 to make an inegrator. It's sloppy but since it's inside the feedback loop, sloppy is OK.

Disconnect the external voltage source driving the VCO and close the loop as shown on the following page:



Be sure the REFCLK frequency is within the range of the VCO's frequency capability.

Display the REFCLK and VCOCLK on the oscilloscope. Change the frequency of the REFCLK input. If the loop is locked, you should see the VCOCLK frequency change accordingly. If it does, your loop is working! Check and see how far you can vary the input clock frequency (high and low) before the loop falls out of lock (this is known as the "lock range").

FM DEMODULATION

If you are able to frequency modulate the REFCLK input, do so. You should then see a demodulated signal at the VCTL input to the VCO. It won't be perfect, since the V-f characteristic of the modulating VCO is probably different from your VCO. But you should see something.

CLOCK FREQUENCY MULTIPLICATION

Going to all this trouble to produce an output frequency that's the same as the input may seem a little underwhelming. Something more interesting is to put a frequency divider in the feedback path, and thereby achieve clock frequency multiplication. Be sure to apply an input frequency low enough so that the multiplied clock frequency is in the range of the VCO's capability.