

ECE4902 C2012 - Lab 7

MOSFET Differential Amplifier

Resistive Load

Active Load

PURPOSE:

The primary purpose of this lab is to measure the performance of the differential amplifier. This is an important topology for integrated applications, which can take advantage of the matching of the MOSFETs in the differential pair. Upon completion of this lab you should be able to:

- Recognize the differential mode and common mode behavior of the differential amplifier.
- Recognize the use of the current mirror as a current source for biasing the differential pair.
- Recognize the use of the current mirror as an active load for increasing the gain the differential pair, and obtaining a single-ended output signal.

LAB 7 - PRELAB

P7-1. For the circuit in Figure L7-1 on the next page, verify that choosing $R_B=30\text{k}\Omega$ gives $I_B\approx 250\mu\text{A}$, and choosing $R_{D1}=R_{D2}=20\text{k}\Omega$ gives output DC bias levels of $V_{O1}\approx V_{O2}\approx +2.5\text{V}$.

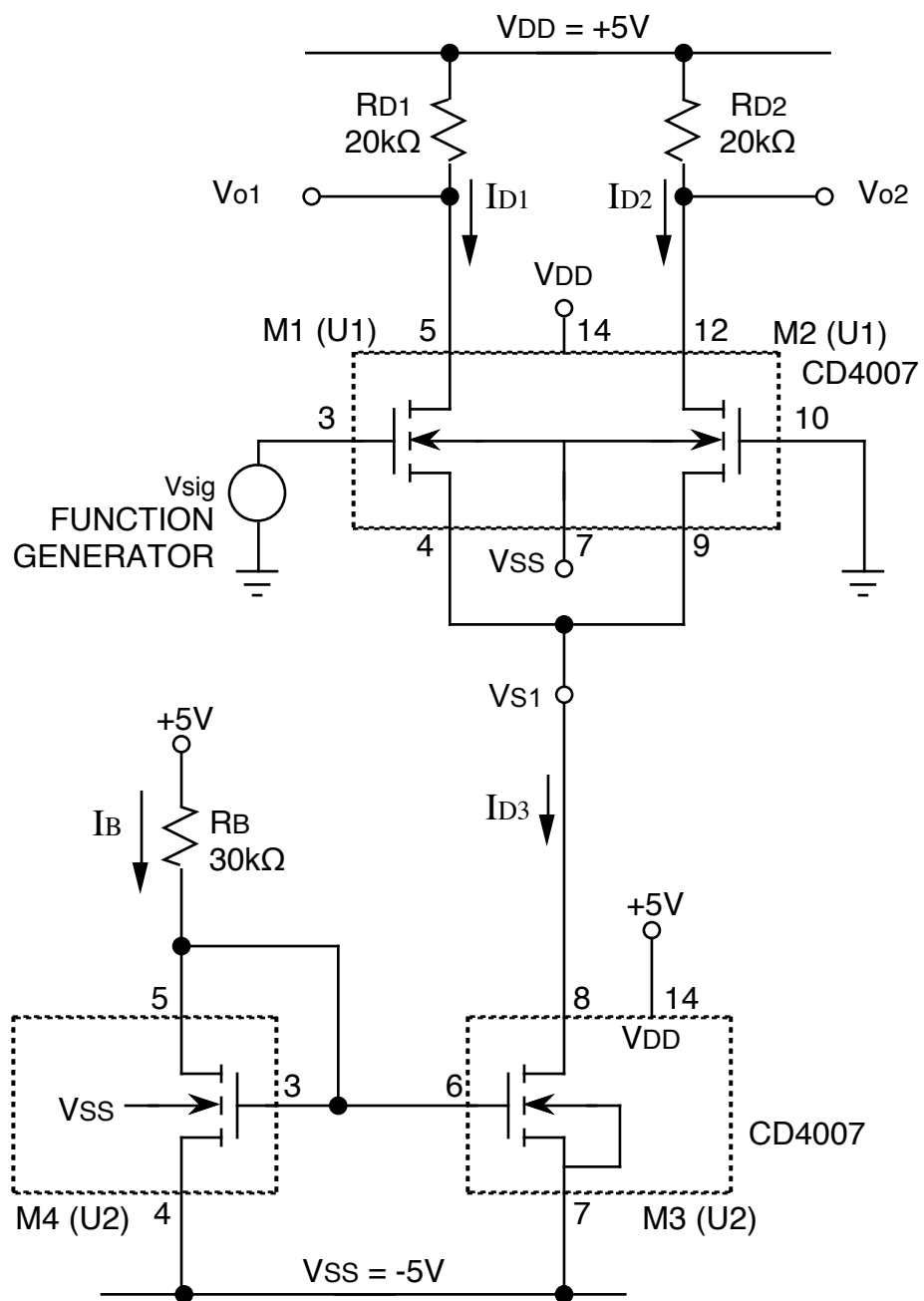


Figure L7-1.

LAB PROCEDURE

DIFFERENTIAL AMPLIFIER

L7-1. Construct the circuit shown in Figure L7-1. Although this circuit will accept differential inputs, we only have a single-ended voltage source. So, one input of the differential amplifier is grounded and the other is driven with the function generator output. Note that no special circuitry or procedures are required to set the DC bias level at the input - since the differential amplifier is biased with a current source, the input can tolerate a wide range of common mode input voltage.

DC BIAS OPERATING POINT

L7-2. The DC bias level at the output is determined by the DC bias current and the value of the load resistors. The current mirror should provide a bias current I_{D3} of about $250\mu\text{A}$. With zero differential input, the bias current should be shared equally by M1 and M2. Resistors R_{D1} and R_{D2} are chosen to achieve a DC bias level of 2.5V at each output.

L7-3. Set the function generator offset and amplitude to zero - you should observe the same DC bias level at each output (zero differential signal). The output difference will not be exactly zero - this is due to a small offset voltage at the input due to imperfect matching between M1 and M2.

From the measured drop across R_{D1} and R_{D2} , calculate the DC bias current in M1 and M2. Also, measure the DC value of V_{GS} for M1 and M2 at the operating point.

DIFFERENTIAL SMALL SIGNAL GAIN

L7-4. With a small triangle wave at the input, measure the small signal gain from input to output. Use a frequency of 1kHz or lower (to make sure that you are below the 3-dB frequency). Measure both the single ended gain (from input to each output separately) and the differential gain (input to total output, $V_{o2} - V_{o1}$). Note that observing the differential output requires the MATH mode on the scope to display the difference of channels; the oscilloscope input is single-ended and cannot measure a differential voltage directly.

Use the 4-channel capability of the scope to also view (in addition to the output voltages) the input voltage v_{in} and V_{S1} , the connected point of symmetry where the sources of the MOSFETs in the differential pair are connected. Note the sign of the gain to each output: inverting for one, noninverting for the other.

DIFFERENTIAL LARGE SIGNAL OUTPUT LIMIT

L7-5. Increase the amplitude on the input until you observe clipping at the output. Measure the positive and negative voltage swing limits, and the input voltage corresponding to each output limit.

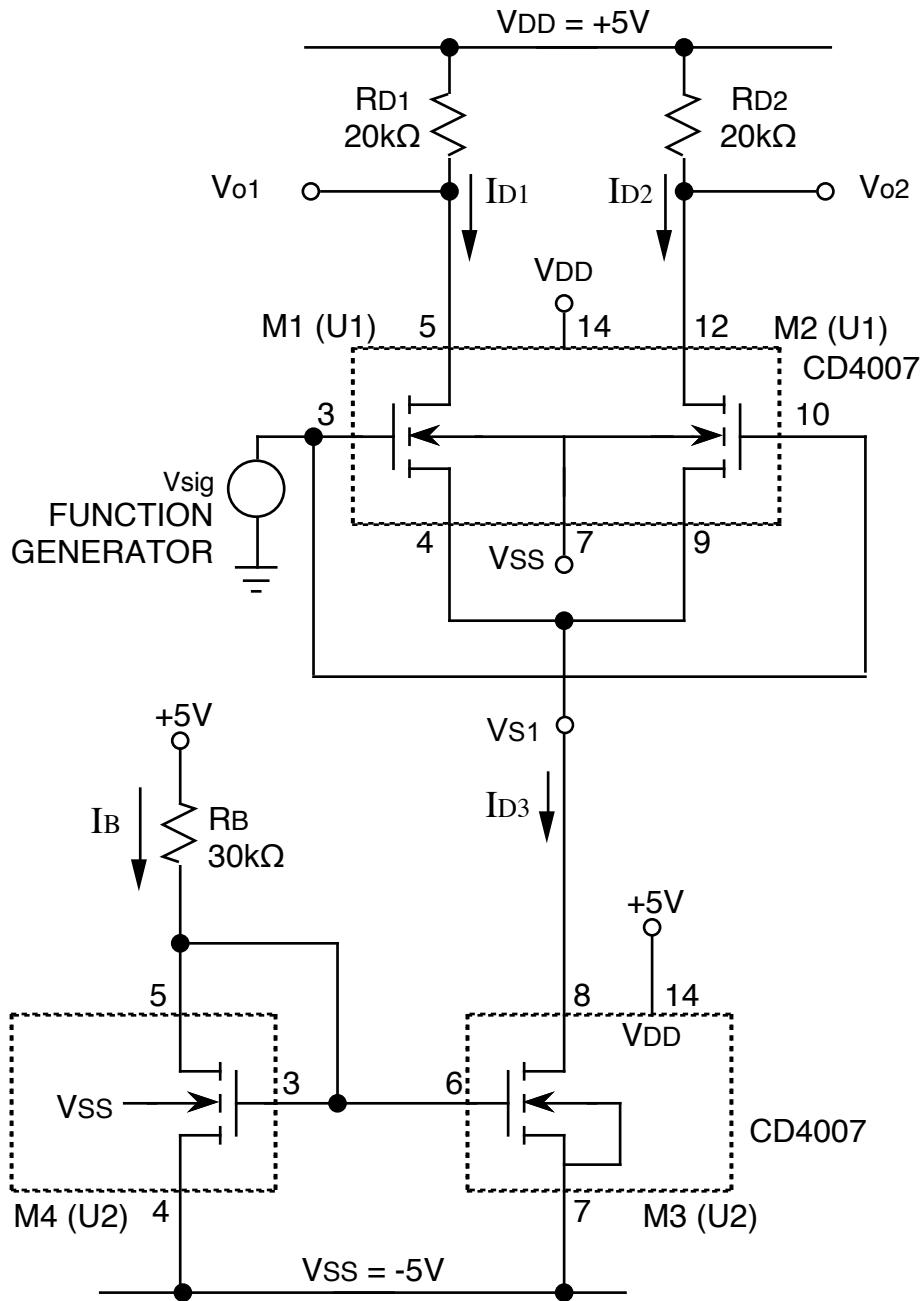


Figure L7-2.
Test for Common Mode response
(Note that differential input = zero)

COMMON MODE REJECTION

L7-6. Connect the input signal to both inputs of the differential amplifier, as shown in Fig. L7-2. Set the amplitude to 1V peak-to-peak. Measure the output amplitude and determine the common mode gain. As in part L7-4, measure both the single ended gain (from input to each output separately) and the gain to the total differential output, $V_{o2} - V_{o1}$. Note that you may need to increase the scope resolution and/or go to AC coupling to see the small amplitude output waveform.

This is “common mode rejection:” compared with the gain for differential signals, the gain should be much lower for common mode (applied “in common” to both inputs) signals.

Use the 4-channel capability of the scope to also view (in addition to the output voltages) the input voltage v_{in} and V_{S1} , the connected point of symmetry where the sources of the MOSFETs in the differential pair are connected. Note that for a common mode input, the voltage at V_{S1} essentially follows the input signal. Thus the current source formed by the M3-M4 mirror sees the input common mode voltage, and there should be a high output impedance at the drain of M3 for good rejection of the common mode input.

COMMON MODE LARGE SIGNAL INPUT LIMIT

L7-7. Increase the input amplitude until the output no longer shows good common mode rejection. Which MOSFETs crash into triode/cutoff?

DIFFERENTIAL AMPLIFIER WITH MIRROR LOAD

L7-8. Construct the circuit shown in Figure L7-3. This is basically the same differential amplifier, with the resistive loads replaced by a P-channel MOSFET current mirror. Note that you will need a third CD4007 package for the current mirror load. Also note the addition of the 100pF capacitor at the output.

LARGE SIGNAL OUTPUT LIMIT

L7-9. Adjust the amplitude and offset on the input until you observe clipping at the output. Measure the positive and negative voltage swing limits, and the corresponding input voltages.

DIFFERENTIAL SMALL SIGNAL GAIN

L7-10. With a small triangle wave at the input, measure the small signal gain from input to output. Reduce amplitude from part L7-9, adjusting offset as you go until the output triangle waveform is within the large signal output limits and reasonably undistorted. Use a frequency of 1kHz or lower (to make sure that you are below the 3-dB frequency). Measure the gain from differential input to the single-ended output, V_{out} .

BANDWIDTH

L7-11. After verifying the undistorted output with the triangle wave from part L7-10, switch to a square wave. Measure the 10%-to-90% rise time, and calculate the bandwidth from the $BW_{tr}=0.35$ relationship. If you have time, check your bandwidth result by changing to a sine wave input and sweeping frequency until the output magnitude has dropped to 0.707 times the low frequency value.

COMMON MODE REJECTION

L7-12. Connect the input signal to both inputs of the differential amplifier, as shown in Fig. L7-2. Set the amplitude to 1V peak-to-peak. Measure the output amplitude and determine the common mode gain. Note that you may need to increase the scope resolution and/or go to AC coupling to see the output waveform, since the common mode gain should be very low.

COMMON MODE LARGE SIGNAL INPUT LIMIT

L7-13. Increase the input amplitude until the output no longer shows good common mode rejection. Which MOSFETs crash into triode/cutoff?

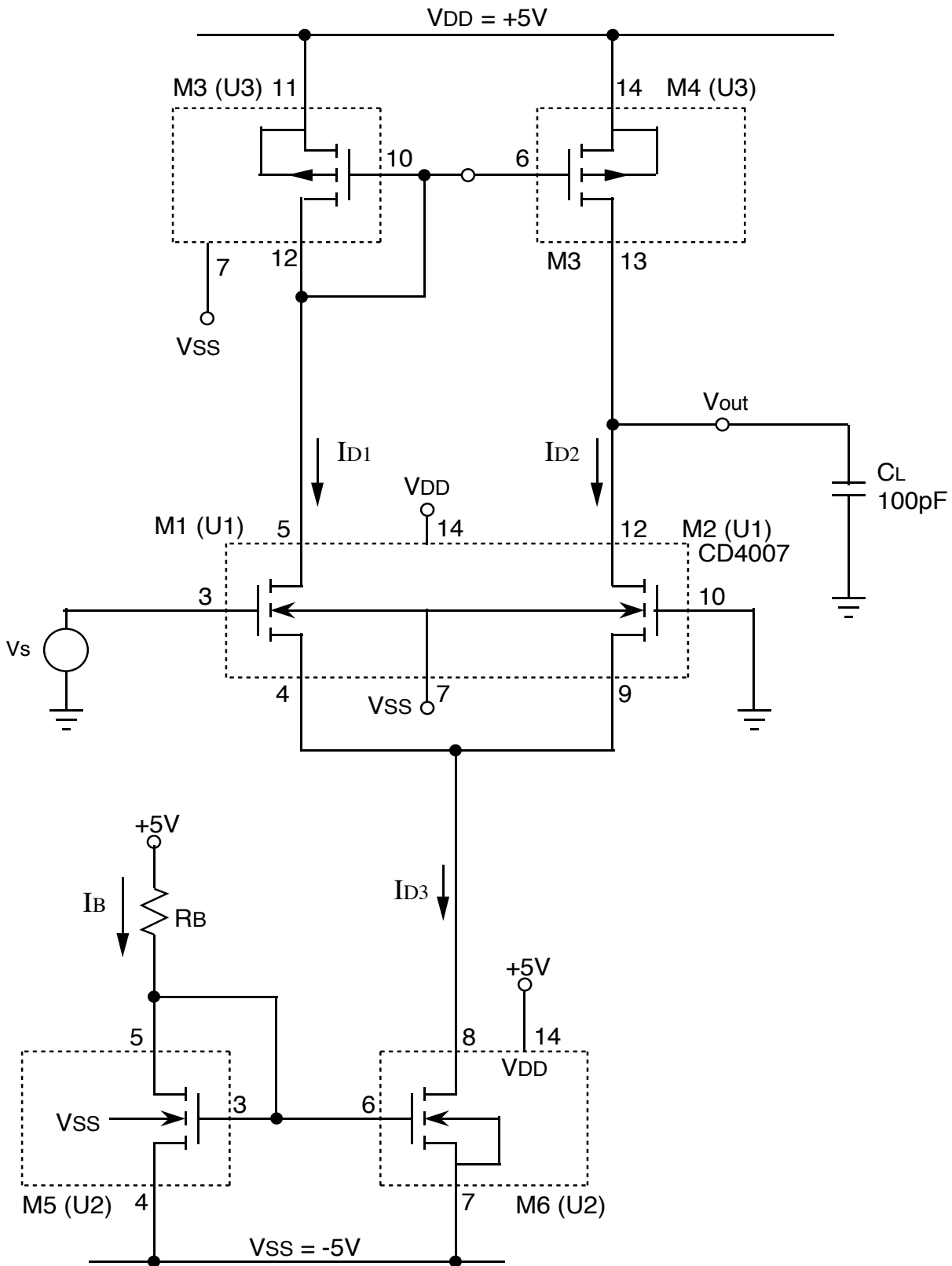


Figure L7-3. Differential amplifier with Active Mirror Load

Lab Writeup

DIFFERENTIAL AMPLIFIER

W7-1. For the circuit of Fig. L7-1: Calculate the expected:

- large signal input-output characteristic (differential input to each output, as well as to the differential output)
- the DC operating point (input voltage corresponding to $V_{O2}-V_{O1}=0V$)
- the small signal gain (slope of the plot at the predicted operating point)
- the large signal output limits

W7-2. Compare the measured operating point value from lab part L7-3 to the predicted value in W7-1.

W7-3. Compare the measured small-signal gain value from lab part L7-4 to the predicted value in W7-1.

W7-4. Compare the measured large signal limits from lab parts L7-5 to the predicted values in W7-1.

W7-5. Explain how and why the differential amplifier rejects common-mode signals (the behavior you should have observed in lab part L7-6).

DIFFERENTIAL AMPLIFIER, ACTIVE LOAD

W7-6. For the circuit of Fig. L7-3: Calculate the expected:

- large signal input-output characteristic (differential input to single-ended output)
- small signal gain (slope of the plot at the predicted operating point)
- bandwidth (3-dB frequency)
- the large signal output limits

W7-7. Compare the measured small-signal gain value from lab part L7-10 to the predicted value in W7-6.

W7-8. Compare the measured bandwidth from lab part L7-11 to the predicted value in W7-6.

W7-9. Compare the measured large signal limits from lab parts L7-9 to the predicted values in W7-6.

W7-10. Compare the small-signal gain of the active load circuit with that of the resistive load circuit.

SIMULATION

S7-1. Using DC and AC sweeps, compare the measured and calculated results from W7-6 through W7-10 to simulated results.