

ECE4902 Lab 9 Extra Credit CMOS OP-AMP WITH CAPACITIVE FEEDBACK

Since CMOS op-amps aren't good at providing the output current necessary for driving resistive loads, very often capacitive feedback is used, as shown in Figure 9-3X. This has several advantages for integrated CMOS applications:

- Avoids wasting power in DC power dissipation of feedback resistors
- Avoids thermal noise of resistors
- Gain can be set more accurately since matching is better for integrated capacitors

One disadvantage is that, with no path for DC current to the - input of the op-amp, there is nothing to define the DC voltage at the - input. Even small leakage currents will eventually cause the voltage at the - input to ramp to one rail or the other, causing large DC errors and eventually exceeding the common mode input range of the op-amp. To get around this problem, some method of defining the DC voltage levels is necessary. In most circuits, a switch is used to periodically force the circuit nodes to a known condition when a known input (such as zero) is applied. In the circuit of Figure 9-3X, the switch is turned "on" when an input of zero is applied. With the switch "on", the amplifier is configured as a follower so the output also goes to zero and the DC voltages on C1 and C2 are defined. Then when the switch is opened, C1 and C2 will hold the correct DC values; any change due to changes from v_{IN} are just superimposed on the DC values. Eventually, leakage currents (slowly) change the DC voltages on C1 and C2 and the DC voltages on C1 and C2 need to be defined again.

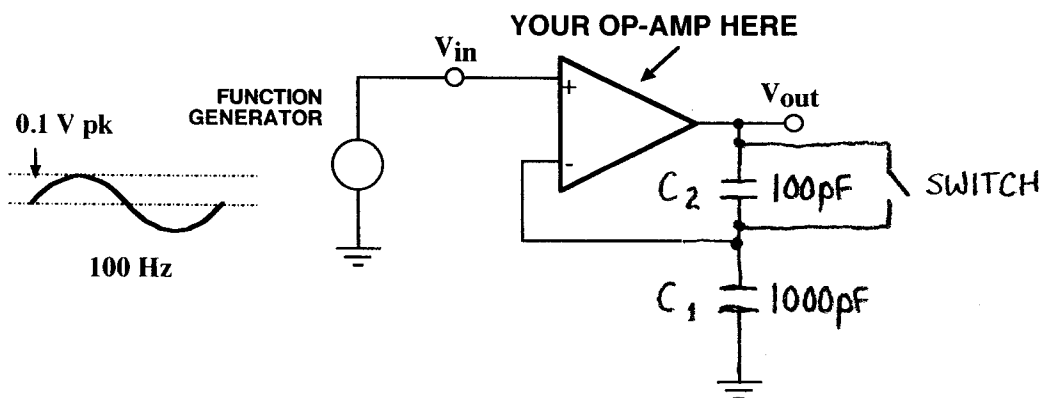


Figure 9-3X.

CLOSED LOOP GAIN OF 11 AMPLIFIER WITH CAPACITIVE FEEDBACK

L9-6X. Configure the op-amp for a gain of 11 as shown in Fig. 9-3X.

To set the DC levels of the circuit correctly, use a short length of wire to short v_{OUT} to v_{IN} when the input amplitude is set to zero. Then remove the short and turn on the input signal source. You may see the output DC level jump when you open the switch ("charge injection") but the DC level should stay within a reasonable range at v_{OUT} . With the input signal source on, you should see a gain to v_{OUT} defined by the capacitor ratio $(1+C1/C2)$.