ECE4902 Lecture 10

2-Stage Op-Amp
Design Example

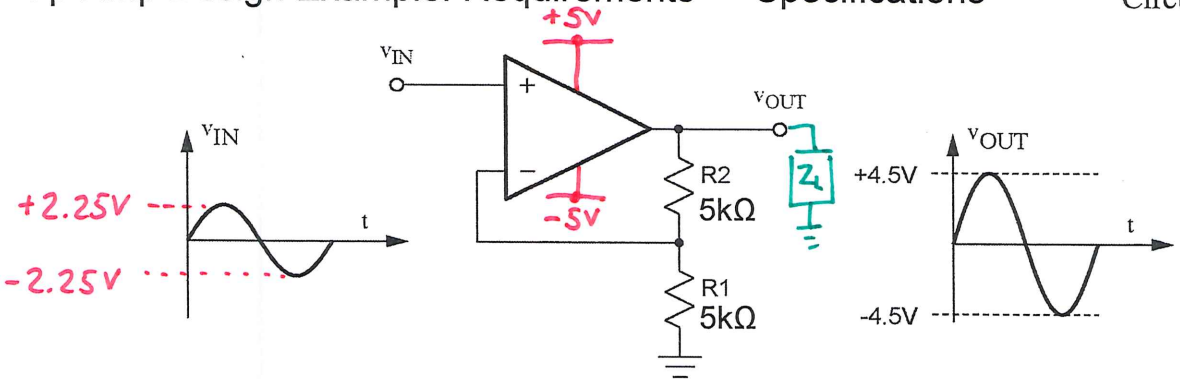
Improving Performance
Cascode

Hand In:
HW 4

Handout:
Design Example

Op-Amp Design Example: Requirements ↔ Specifications

Circuit design: Choose architecture
Specify W, L for all MOSFETs;
R, C values



Circuit level:
Op-amp Specification:

System Level
Requirements:
(Audio application)
Precision

Gain = 2;
feedback resistors 5kΩ

Supplies: +/- 5V;
output V swing +/- 4.5V

Frequency response:
-1dB down at 100kHz

f_{3dB} = ? 194 kHz

No distortion from
Slew Rate Limiting

DISTORTION
(NONLINEARITY)

Output voltage limit
± 4.5 V

Input Common Mode Range
± 2.25 V $V_{ICM} = \frac{V_+ + V_-}{2} \approx \frac{V_{OUT}}{2}$

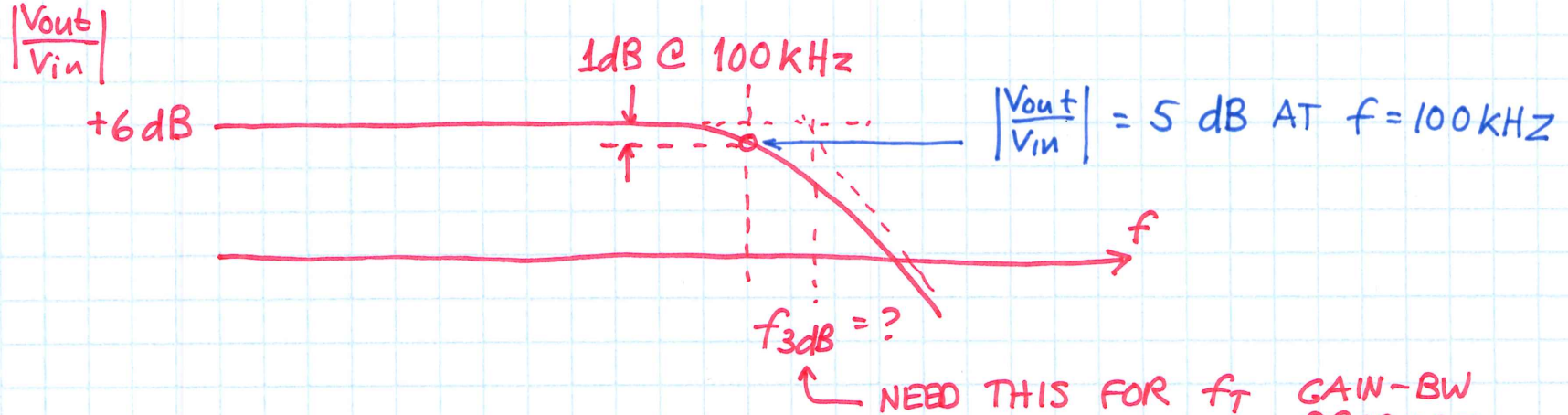
Gain-bandwidth product f_T
388 kHz 2 × 194 kHz

Slew Rate
2.83 V/μsec

Maximum output current
± 450 μA $\frac{\pm 4.5V}{10k\Omega}$

DC Open Loop Gain A_0
2000

WHAT CLOSED LOOP f_{3dB} DO WE NEED? CLOSED LOOP TRANSFER FUNCTION



$$\frac{V_{out}}{V_{in}} = \frac{2}{1 + j\left(\frac{f}{f_{3dB}}\right)}$$ } DC GAIN; } CLOSED LOOP 3dB FREQUENCY

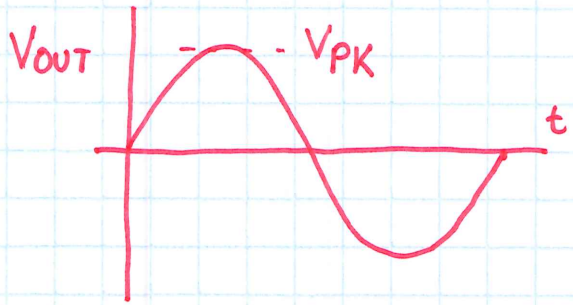
CONVERT 5 dB TO NUMBER: $dB \quad 20\log_{10}\underbrace{\left(\frac{V_{out}}{V_{in}}\right)}_{5} \Rightarrow \frac{V_{out}}{V_{in}} = 10^{(5/20)} = 1.778$

AT 100 kHz:

$$1.778 = \frac{2}{\sqrt{1 + \left(\frac{100\,kHz}{f_{3dB}}\right)^2}} \Rightarrow \left(\frac{1.778}{2}\right)^2 = \frac{1}{1 + \left(\frac{100\,kHz}{f_{3dB}}\right)^2}$$

$$\left(\frac{100\,kHz}{f_{3dB}}\right)^2 = 0.265 \Rightarrow f_{3dB} = 194\ kHz$$

SLEW RATE: MAXIMUM dV_{OUT}/dt



$$V_{OUT} = V_{PK} \sin(2\pi f t)$$

$$\frac{dV_{OUT}}{dt} = 2\pi f V_{PK} \underbrace{\cos(2\pi f t)}_{\text{MAX } 1}$$

$$\left.\frac{dV_{OUT}}{dt}\right|_{MAX} = \underbrace{2\pi f}_{100\text{kHz}} \overbrace{V_{PK}}^{\text{MAX}}{}_{4.5\text{V}}$$

GOAL (COULD RELAX)

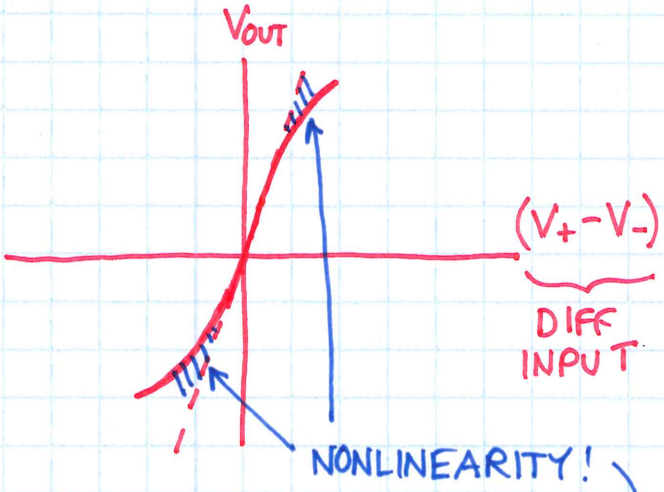
$$\text{SLEW RATE} = 2\pi (100\,\text{kHz})(4.5\,\text{V})$$

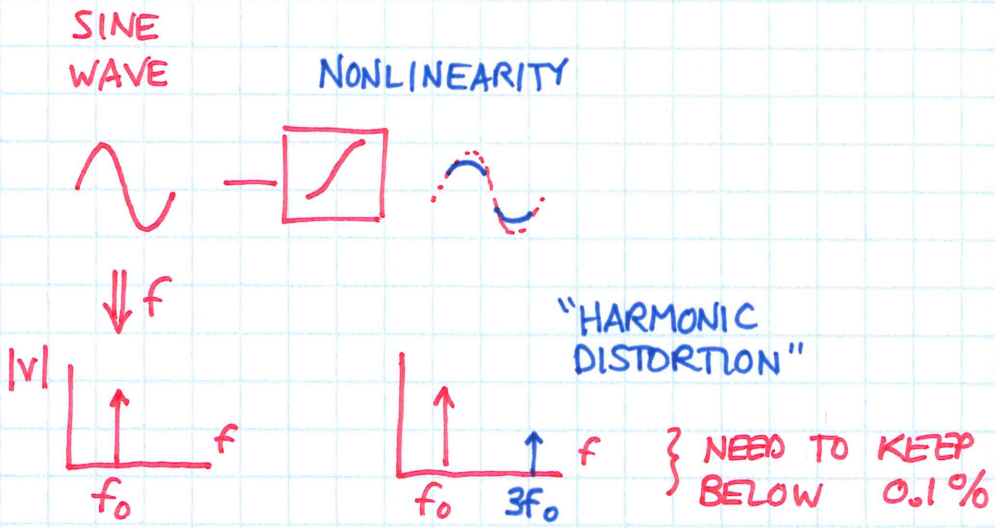
$$= 2.83\ \text{V}/\mu\text{sec} \quad \text{(GOAL)}$$

FALLBACK (20 kHz)

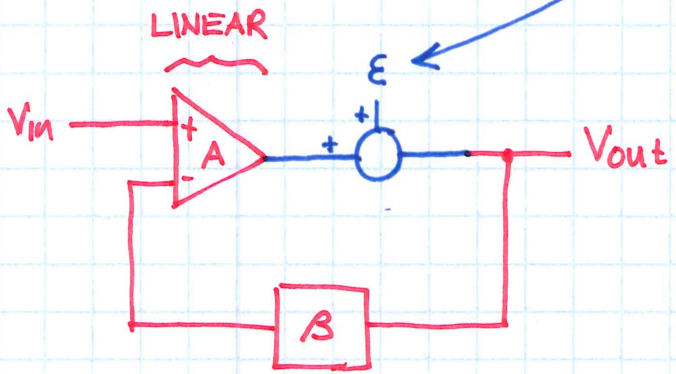
$$2\pi (20\,\text{kHz})\, 4.5\,\text{V} = 0.57\ \text{V}/\mu\text{sec}$$

OPEN LOOP GAIN VS. LINEARITY, DISTORTION





MODEL WITH FEEDBACK



$$V_{out} = \varepsilon + A(V_{in} - \beta V_{out})$$

$$V_{out} = \varepsilon + A V_{in} - A\beta V_{out}$$

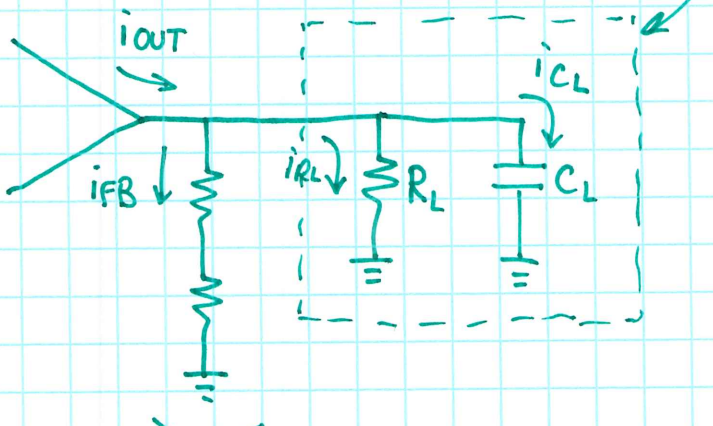
$$V_{out}(1 + A\beta) = \varepsilon + A V_{in}$$

$$V_{out} = \underbrace{\left(\frac{A}{1+A\beta}\right) V_{in}}_{\text{WANT}} + \underbrace{\left(\frac{1}{1+A\beta}\right)}_{\text{MORE } A\beta \text{ REDUCES EFFECT OF } \varepsilon \text{ DISTORTION}} \varepsilon$$

$$V_{out} = (\quad) V_{in} + \underbrace{(\quad)}_{\text{WANT THIS}} \varepsilon$$

$$\underbrace{\leq 0.001}_{(0.1\%)} = \frac{1}{1 + A\left(\frac{1}{2}\right)} \Rightarrow A > 2000$$

EFFECT OF LOAD IMPEDANCE Z_L



$R_{FB(TOTAL)}$

RESISTIVE

$R_{FB(TOTAL)} \| R_L$

CAPACITIVE PART:

$$i_C = C_L \frac{dV_{OUT}}{dt}$$

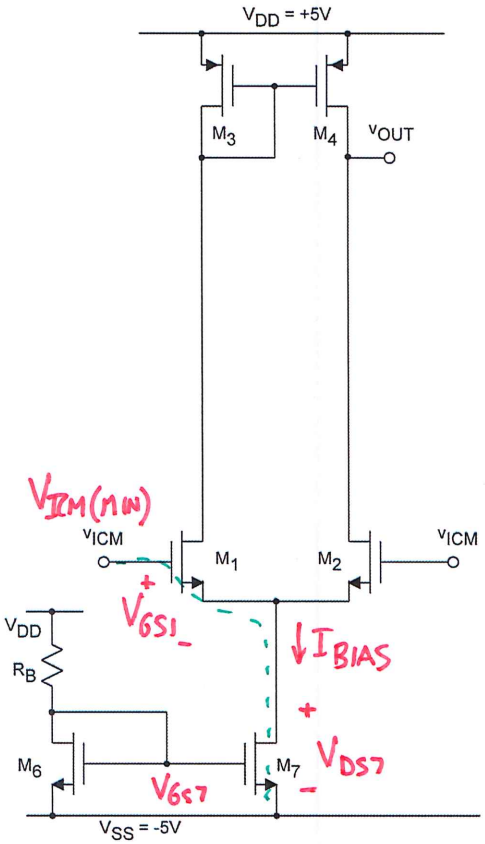
CAREFUL! MAY EXCEED RESISTIVE CURRENT AT HIGH FREQUENCIES

GENERAL PURPOSE OP-AMP

MINIMUM TOTAL R_L

MAXIMUM C_L

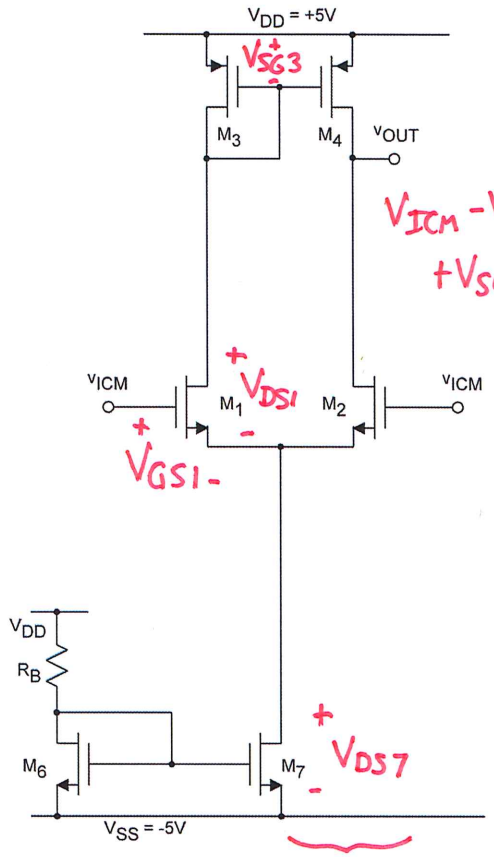
Op-amp input common mode (CM) range limits: NEED TO HAVE ALL DEVICES IN SATURATION (NO TRIODE CRASH!)



M_7 TRIODE CRASH:
(I_{BIAS} DECREASES)

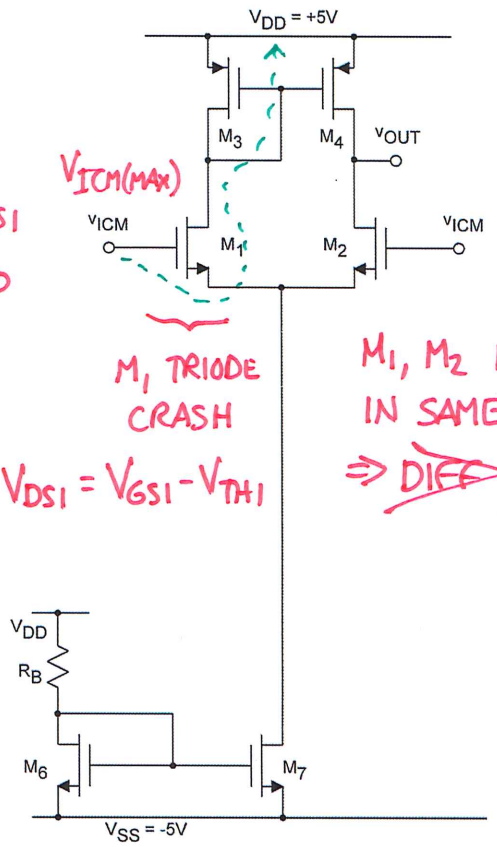
$V_{ICM(MIN)} - V_{GS1} - V_{GS7} = -5V$

$V_{GS7} - V_{TH7}$
AT TRIODE CRASH



$V_{ICM} - V_{GS1} + V_{DS1} + V_{SG3} = V_{DD}$

$V_{DS7} = V_{ICM} - V_{GS1}$



M_1 TRIODE CRASH

$V_{DS1} = V_{GS1} - V_{TH1}$

M_1, M_2 NO LONGER IN SAME OP REGION

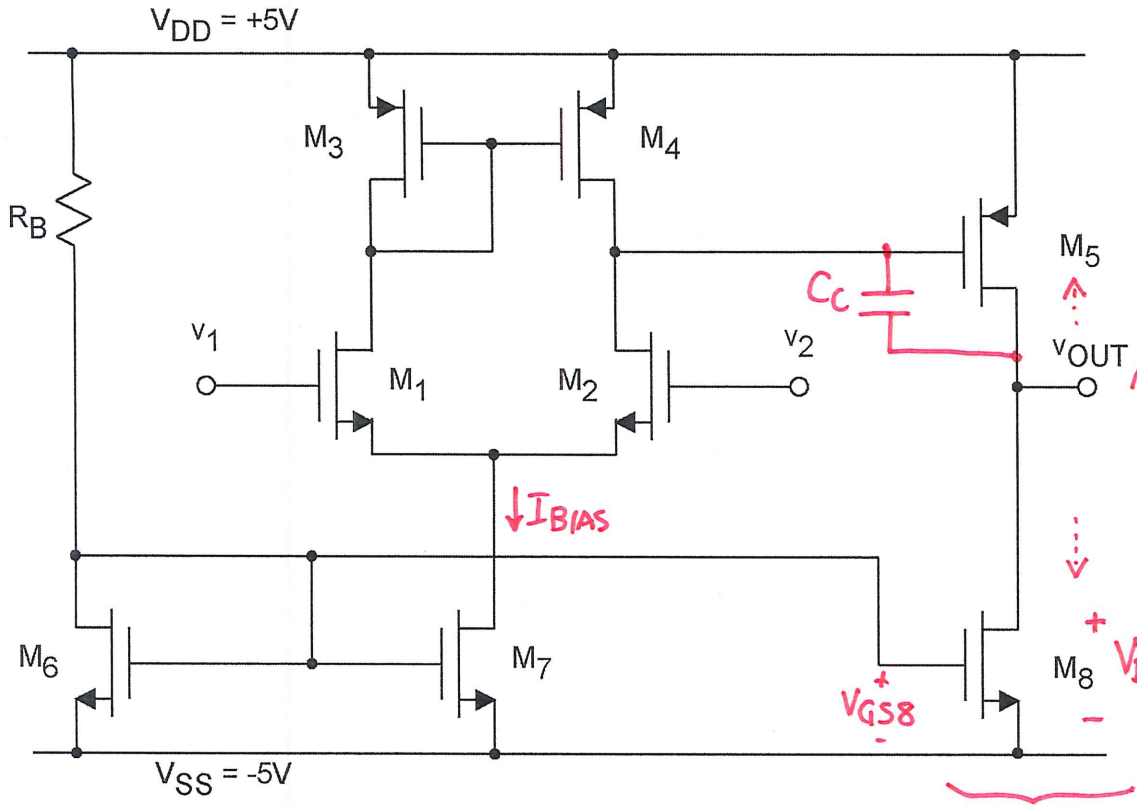
⇒ ~~DIFF PAIR~~

Op-Amp Design Example: Specifications ⇔ MOSFETs ?

W, L, I_D, V_{GS}

~~32 UNKNOWNS~~

~~32 EQ?~~



g_M

ACTIVE:
$V_{DS8} > V_{GS8} - V_{TH}$

CONSIDERATIONS:
- ALL DEVICES IN ACTIVE REGION
  LIMITS ⇔ TRIODE CRASH

f_T (DOMINANT POLE MODEL): $\frac{g_{m1}}{2\pi C_C}$

$SR = \frac{I_{BIAS}}{C_C}$

WHICH MOSFETS?

Op-amp Specification:

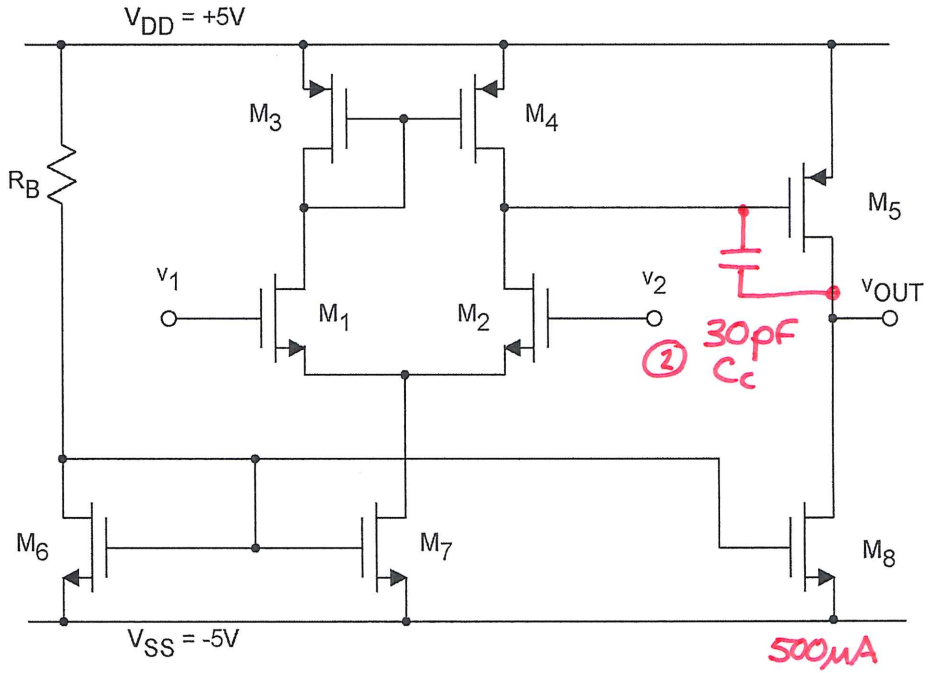
Output voltage limit ↑	M5
Output voltage limit ↓	TRIODE CRASH M8
Input Common Mode Range ↑	M1 M3
Input Common Mode Range ↓	M1 M2 M7
Gain-bandwidth product f_T	M1 M2 — C_C
Slew Rate	M7 — C_C
Maximum output current SOURCE	M5
Maximum output current SINK	M8
DC Open Loop Gain A_0	M1 M2 M4 M5 M8

$g_{mI}(r_{o2} \| r_{o4})\, g_{mII}(r_{o5} \| r_{o8})$

JUST MAKE SURE THIS IS BIG!

Specifying Op-Amp Design:

MOSFET	DC Bias		Size (1)		Remarks
	ID [µA]	$V_{GS} - V_{TH}$	W [µm]	L [µm]	
M1				10	
M2				10	
M3				10	
M4				10	
M5	500mA (4)	−0.4V (5)	7200	10	
M6		0.4V		10	
M7		0.4V		10	
M8	500mA (3)	(4) 0.4V	(5) 2400	10	



Parameter	N-channel	P-channel	Units
V_{TH}	+1.90	-1.60	V
μC_{ox}	2.6E-5	9.1E-6	A/V^2
λ (L=10µm)	0.05	0.028	V^{-1}

① MINIMIZE AREA (CD4007 PARAMETERS) ALL $L = 10\mu m$
(COULD CHANGE LATER; HAVE TO START SOMEWHERE!)

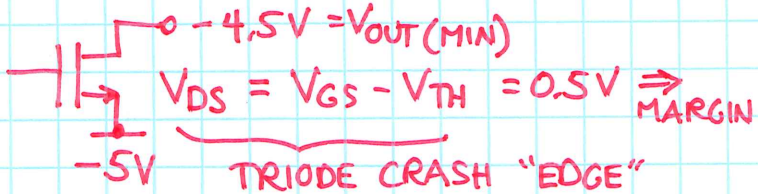
② CHOOSE $C_c = 30\,pF$ [SEE ECE529C; NOISE CONSIDERATIONS]

③ M_8 MUST ALWAYS CONDUCT MAX CURRENT

$450\mu A \Rightarrow 500\mu A = I_{D8}$

④ OUTPUT SWINGS DETERMINED BY TRIODE CRASH

M_8:



SAME FOR M_5

PMOS: $-0.4V$

⑤ W_8 FROM SQUARE LAW

$$500\mu A = \frac{2.6E\text{-}5}{2}\frac{W}{10}(0.4V)^2 \Rightarrow 2400\mu m$$

W_5

$$500\mu A = \frac{9.1E\text{-}6}{2}\frac{W}{10}(-0.4V)^2 \Rightarrow 7200\mu m$$