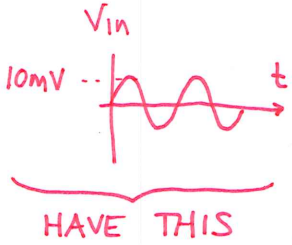
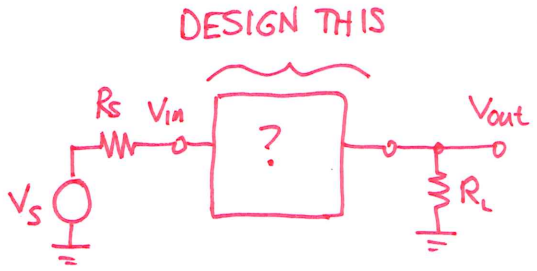
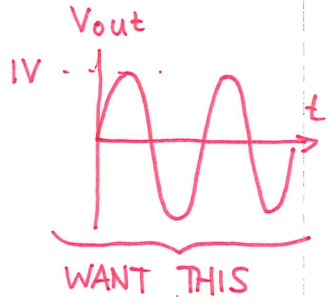
ECE4902 Lecture 1

Administrative Information
Design example: Audio amplifier
ECE3204 Review
Discrete vs. Integrated Design
ECE4904 "Review"
p-n Junction
MOSFET

Handouts:
Administrative Information
Op-Amp Errors (ECE3204 Review)
IC Op-amp Introduction
ECE4904 "Review"
p-n Junction
MOS Symbols / Cross Section View



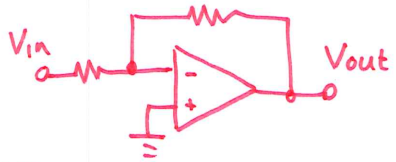


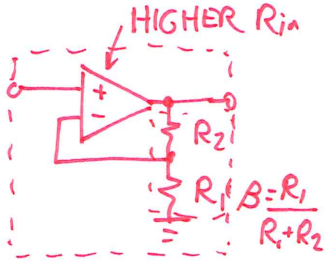


DESCRIBE WHAT WE WANT [?] TO DO:

QUALITATIVE

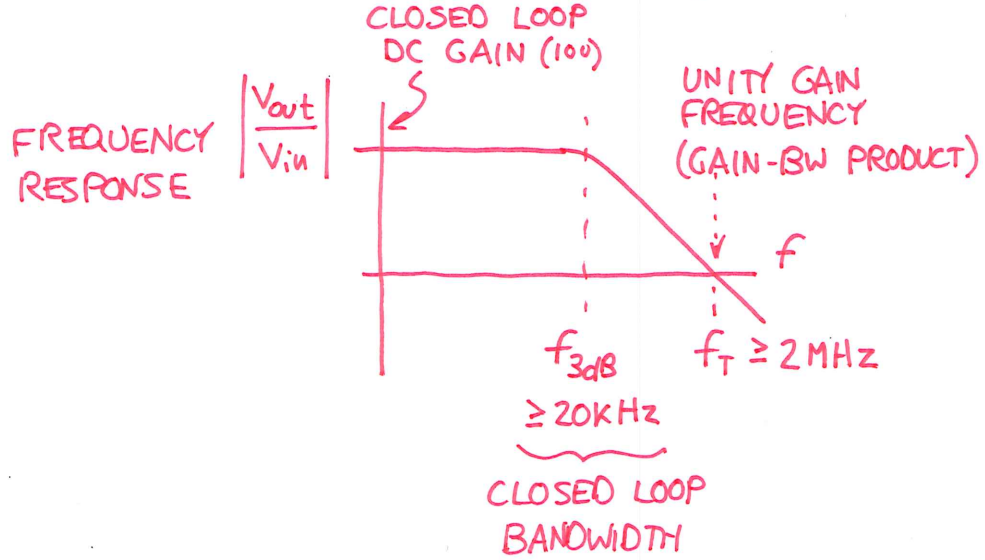
- ☑ AMPLIFY (SCALE UP) V_{in}
- ☑ LINEAR AMPLIFICATION (NO DISTORTION)
- ☑ FLAT FREQUENCY RESPONSE (AUDIO 20Hz-20kHz)
- → NEED TO TRANSLATE TO QUANTITATIVE REQUIREMENTS



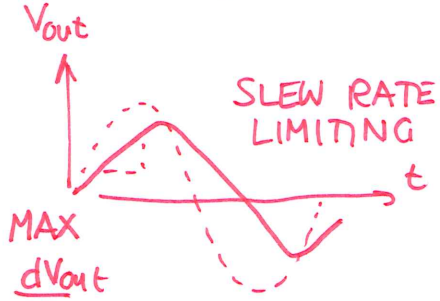


GAIN NEEDED:

$$\frac{out}{in} = \frac{1V}{10mV} = +100 \underbrace{\frac{R_1+R_2}{R_1}}$$



DISTORTION : SUPPLY CLIPPING (V_{DD} SUPPLIES)



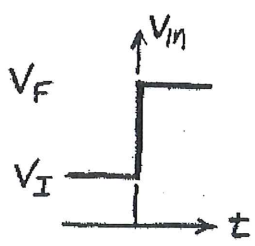
$$SR \geq 2\pi f_{MAX} V_{outMAX}$$

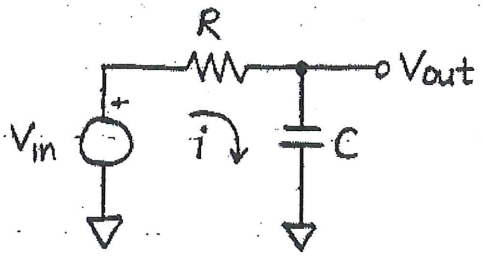
Op-Amp Errors

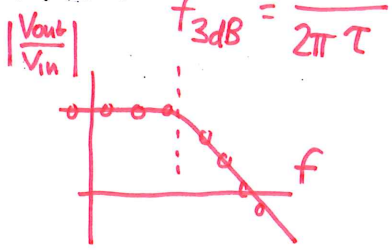
		Static (DC)	Dynamic (AC)
Linear	Error Source	*Offset Voltage* *DC Bias Current*	*Finite Bandwidth*
	Text	Sec. 9.1, 13.2	Sec. 8.1, 9.1
	Analysis Strategy	1. Add DC sources to ideal op-amp to model errors 2. Analyze with superposition to find contribution of each error source to output voltage 3. Add in "worst case" fashion • Offset voltage can be either polarity • Bias current polarity known from type of op-amp input stage	Model closed loop behavior with first-order transfer function: • DC gain from ideal op-amp assumptions • Closed loop bandwidth (3-dB frequency) $f_{3\text{-dB}}$ from gain-bandwdith product relationship Gain-bandwidth product procedure: 1. Redraw circuit with all inputs suppressed (set = 0) 2. Find feedback factor β (fraction of output fed back to inverting input) 3. Closed loop bandwidth $f_{3\text{-dB}}$ will be unity gain frequency f_t mutliplied by β
Non-Linear	Error Source	*Output voltage swing limit* *Output current limit*	*Slew rate limit*
	Text	Sec. 9.1	Sec. 9.8, 10.5.1
	Analysis Strategy	1. Determine maximum total v_{OUT}, i_{OUT}, excursion at op-amp output from linear system model 2. Compare maximum, minimum to op-amp limits	1. Determine $v_{OUT}(t)$ from linear system behavior (transfer function for sine wave, general exponential response for step) 2. Calculate time derivative $dv_{OUT}(t)/dt$ 3. Compare maximum positive and negative $dv_{OUT}(t)/dt$ to op-amp slew rate limit

Textbook: Razavi, *Design of Analog CMOS Integrated Circuits*

STEP RESPONSE OF FIRST ORDER SYSTEM







First order differential equation for V_{out}

$$\underbrace{V_{out} = V_{in} - iR}_{\text{KVL}} \Rightarrow \underbrace{i = C\frac{d}{dt}V_{out}}_{\text{CAPACITOR}} \Rightarrow \frac{d}{dt}V_{out} = \left(\frac{-1}{RC}\right)V_{out} + \left(\frac{1}{RC}\right)V_{in}$$

Solve differential equation; homogeneous solution: $V_{in}=0$
try solution of form $Ae^{-t/\tau}$; substitute

$$\frac{d}{dt}\left[Ae^{-t/\tau}\right] = \left(\frac{-1}{RC}\right)\left[Ae^{-t/\tau}\right]$$

$$\frac{-1}{\tau}Ae^{-t/\tau} = \frac{-1}{RC}Ae^{-t/\tau} \Rightarrow \tau = RC \quad \left\{\text{"TIME CONSTANT"}\right.$$

Particular solution: when output is constant,
$t \to \infty$, $dV_{out}/dt \to 0$; try constant solution $V_{out} = B$
As $t \to \infty$, $V_{in} = V_F$

$$\left(\frac{-1}{RC}\right)B + \left(\frac{1}{RC}\right)V_F = 0 \Rightarrow B = V_F$$

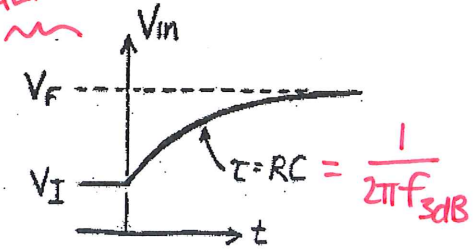
Boundary condition: at $t=0$, $V_{out} = V_I$ (voltage across C cannot change instantaneously)

$$Ae^{-0/\tau} + V_F = V_I \Rightarrow A = V_I - V_F$$

General solution:

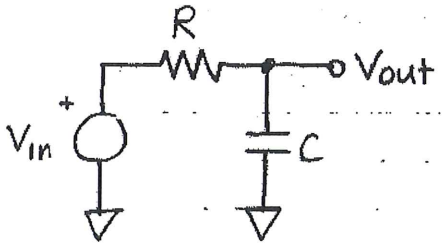
$$\boxed{V_{out}(t) = V_F - (V_F - V_I)e^{-t/RC}} \qquad \tau = RC$$

DC ANALYSIS



BANDWIDTH AND RISETIME

Consider the single pole network



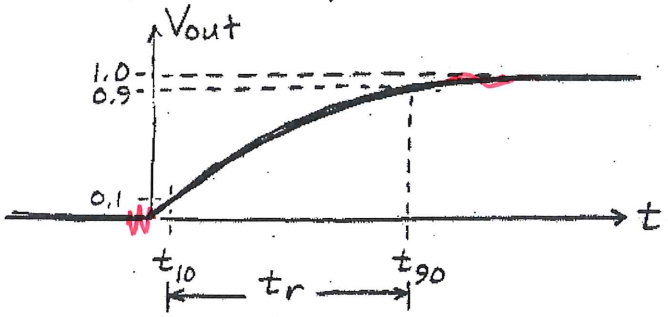
$$\frac{V_{out}}{V_{in}} = H(s) = \frac{1}{1+sRC} = \frac{1}{1+s\tau}$$

Letting $s = j\omega$, we have

$$H(j\omega) = \frac{1}{1+j\omega\tau} = \frac{1}{1+j\left(\frac{\omega}{\omega_0}\right)}$$

where $\omega_0 = 1/\tau$ is the 3dB bandwidth, in radians/sec

The "rise time" t_r is defined as the time required for the output to rise from 10% to 90% of the output step:



From general step response

$$0.1 = 1.0 - e^{-t_{10}/\tau} \Rightarrow t_{10} = -\tau \ln(0.9)$$
$$0.9 = 1.0 - e^{-t_{90}/\tau} \Rightarrow t_{90} = -\tau \ln(0.1)$$
$$t_r = t_{90} - t_{10} = \tau \ln(9)$$

Or, $\boxed{t_r = 2.2\tau}$

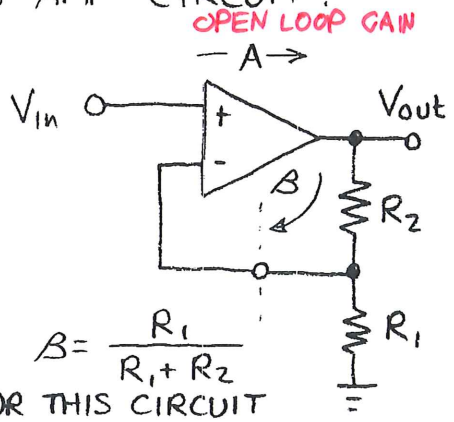
Since $\tau = 1/\omega_0$, and $f_0 = \omega_0/2\pi = BW$ (3dB bandwidth in Hz)

$$t_r = 2.2\frac{1}{\omega_0} = \frac{1}{BW}\frac{2.2}{2\pi} \Rightarrow \boxed{BW \cdot t_r = 0.35}$$

Approximately valid for any linear system with poles near real axis (little overshoot in step response)

OP-AMP AS A CLASSICAL FEEDBACK SYSTEM

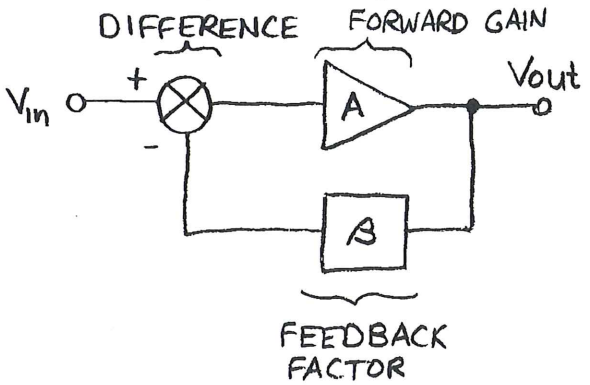
OP-AMP CIRCUIT:



$$\beta = \frac{R_1}{R_1 + R_2}$$

FOR THIS CIRCUIT

CLASSICAL FEEDBACK:



β: "FEEDBACK FACTOR" FRACTION OF V_{out} FED BACK TO V_-

FIND CLOSED LOOP GAIN $G = \frac{V_{out}}{V_{in}}$

$$V_{out} = A(V_{in} - \beta V_{out}) \Rightarrow \boxed{\frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta} = G}$$

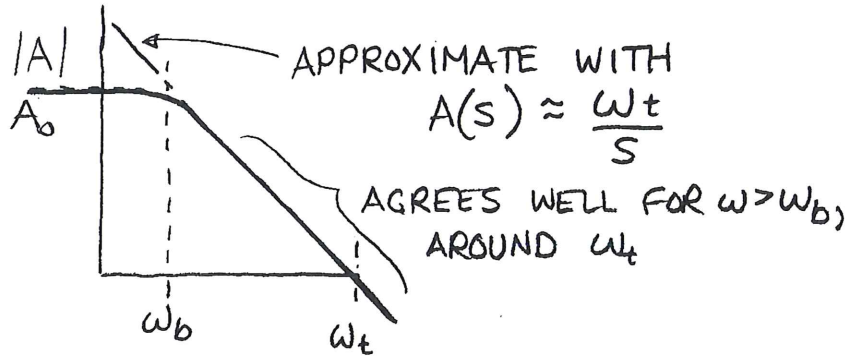
✓AS EXPECTED

$G \to \frac{1}{\beta}$ AS $A \to \infty$

WHAT IS CLOSED LOOP GAIN G WHEN A IS FINITE?
REAL OP-AMP HAS SINGLE POLE TRANSFER FUNCTION

$$A = A(s) = \frac{A_0}{1 + \frac{s}{\omega_b}}$$

OPEN LOOP GAIN VS. ω



SUBSTITUTE IN G EXPRESSION

$$G = \frac{A}{1 + A\beta} = \frac{\frac{\omega_t}{s}}{1 + \beta\frac{\omega_t}{s}}$$

MULTIPLY NUM, DEN BY $\frac{s}{\beta\omega_t}$

MASSAGE INTO GENERAL FIRST ORDER FORM

$$G = \frac{[\text{DC GAIN}]}{1 + \frac{s}{[\omega_{3dB}]}}$$

$$G = \frac{\frac{\omega_t}{s}\,\frac{s}{\beta\omega_t}}{\left(1+\beta\frac{\omega_t}{s}\right)\frac{s}{\beta\omega_t}} \Rightarrow \boxed{\frac{\frac{1}{\beta}}{1+\frac{s}{\beta\omega_t}}}$$

$\frac{1}{\beta}$ } DC GAIN

$1+\frac{s}{\beta\omega_t}$ } CLOSED LOOP BANDWIDTH ω_{3dB}

GAIN-BANDWIDTH TRADEOFF!:

WHEN WE CHOOSE A FEEDBACK FACTOR β (FRACTION <1)

TO GET A CLOSED LOOP DC GAIN OF $\frac{1}{\beta}$

CLOSED LOOP BANDWIDTH ω_{3dB} IS $\beta\omega_t$

UNITY GAIN FREQUENCY ω_t REDUCED BY β FACTOR

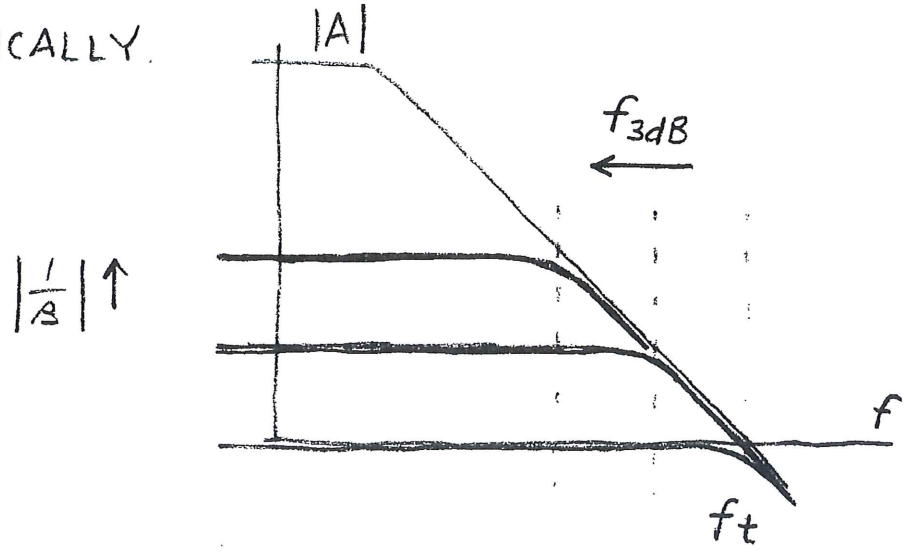
INVERSE RELATIONSHIP: PRODUCT IS CONSTANT

[CLOSED LOOP GAIN]	×	[CLOSED LOOP BANDWITH]	=	[GAIN-BANDWIDTH PRODUCT]
$\frac{1}{\beta}$		$\underbrace{\beta\omega_t}_{\omega_{3dB}}$		$\underbrace{\omega_t}_{\text{UNITY GAIN FREQUENCY}}$

FOR LM741, $f_t = 1$ MHz

FOR LF356, $f_t = 4$ MHz

GRAPHICALLY

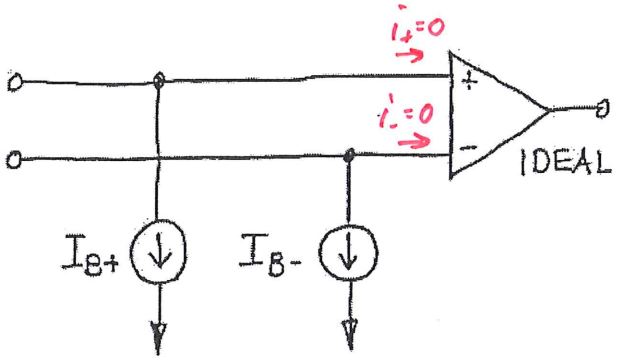


EE3204
DC ERRORS

OFFSET VOLTAGE
Model as a source in series with either input of an ideal op-amp:

V_{os} can be of either + or - sign

BIAS CURRENT
Model as a current source in parallel with each input of an ideal op-amp:

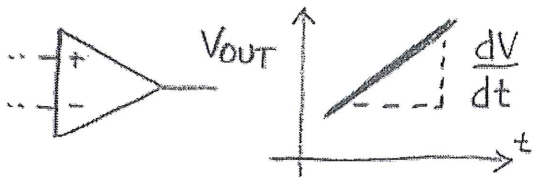


Polarity of I_B is usually known (depends on type of transistors in op-amp input stage)

ANALYSIS
Use superposition and ideal op-amp assumptions to simplify analysis.

SLEW RATE LIMITING

WHAT IT IS:



MAXIMUM dV/dt POSSIBLE AT OP-AMP OUTPUT

"SPEED LIMIT"

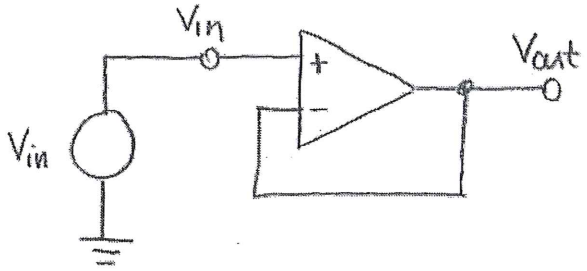
ANALYSIS PROCEDURE

1) DETERMINE OUTPUT $V_{OUT}(t)$ FROM LINEAR BEHAVIOR (TRANSFER FUNCTION, 1ST ORDER STER RESPONSE)

2) CALCULATE $dV_{OUT}(t)/dt$

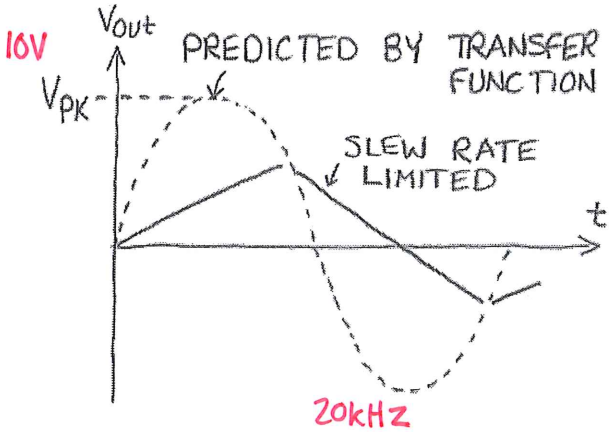
3) SEE IF MAX $dV_{OUT}(t)/dt$ EXCEEDS SLEW RATE LIMIT

EXAMPLE: LM741



LM741
SLEW RATE LIMIT
$0.5 \frac{V}{\mu sec}$

SINUSOID



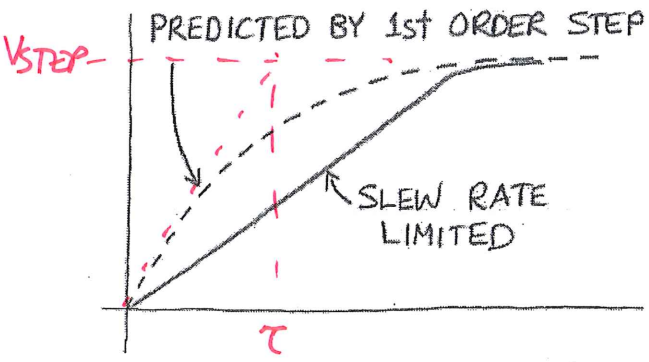
$$V_{out}(t) = V_{PK} \sin(2\pi f t)$$

$2\pi f$ 10V

$$\frac{dV_{out}(t)}{dt} = 2\pi f V_{PK} \cos(2\pi f t)$$

MAX $\frac{dV}{dt}$ = 1.2 V/msec MAX = 1

STEP



$$V_{out}(t) = V_F - (V_F - V_I) e^{-t/\tau}$$

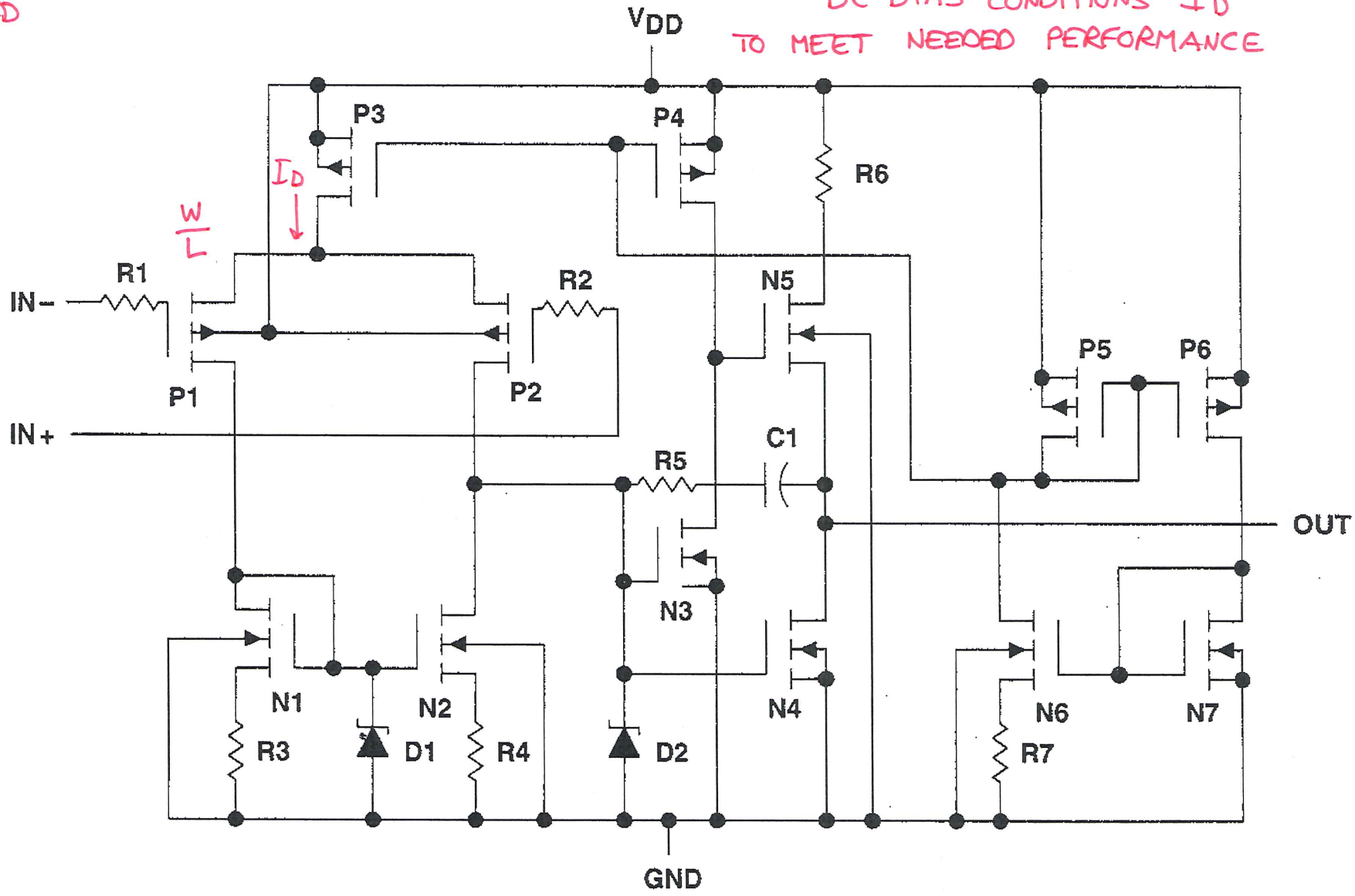
$$\frac{dV_{out}(t)}{dt} = \frac{(V_F - V_I)}{\tau} e^{-t/\tau}$$

MAX $\frac{dV}{dt}$ MAX = 1 at t = 0

equivalent schematic (each amplifier)

SIMPLIFIED

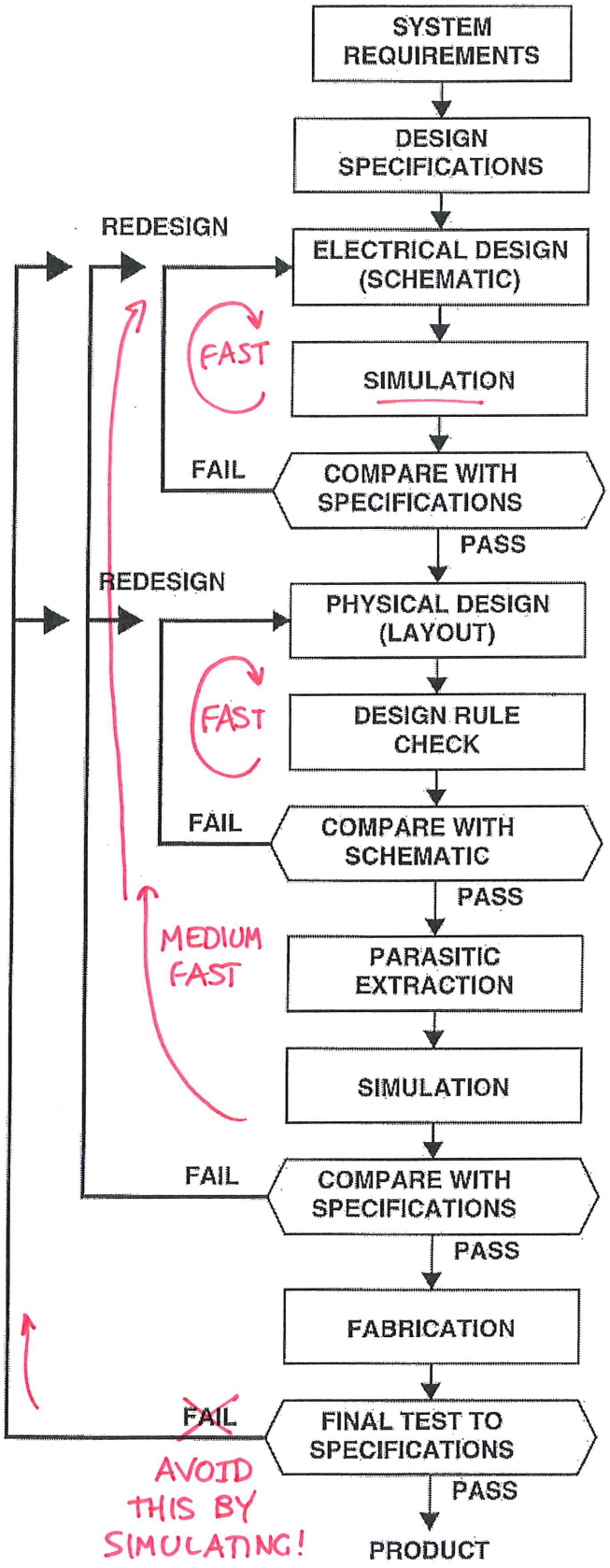
ECE4902: CHOOSE MOSFET SIZES $\frac{W}{L}$ DC BIAS CONDITIONS I_D TO MEET NEEDED PERFORMANCE



Discrete vs. Integrated circuit design

Discrete	Integrated
- Board-level system	+ Chip-level system
- Devices "Take what you get"	+ Control over device geometry
- Matching difficult	+ Matching inherent
+ Precise values possible	- Absolute values vary widely
+ Large R, C possible	- Largest C ≈ 100pF; large R bad
+ Many types of components	- Limited to types in process
+ Possible to breadboard	- Can't breadboard; simulation

EE4902 ANALOG IC DESIGN FLOW

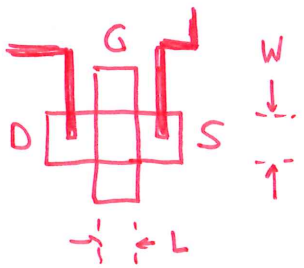


QUALITATIVE

QUANTITATIVE

CHOOSE OP-AMP ARCHITECTURE

SPICE (Cadence)

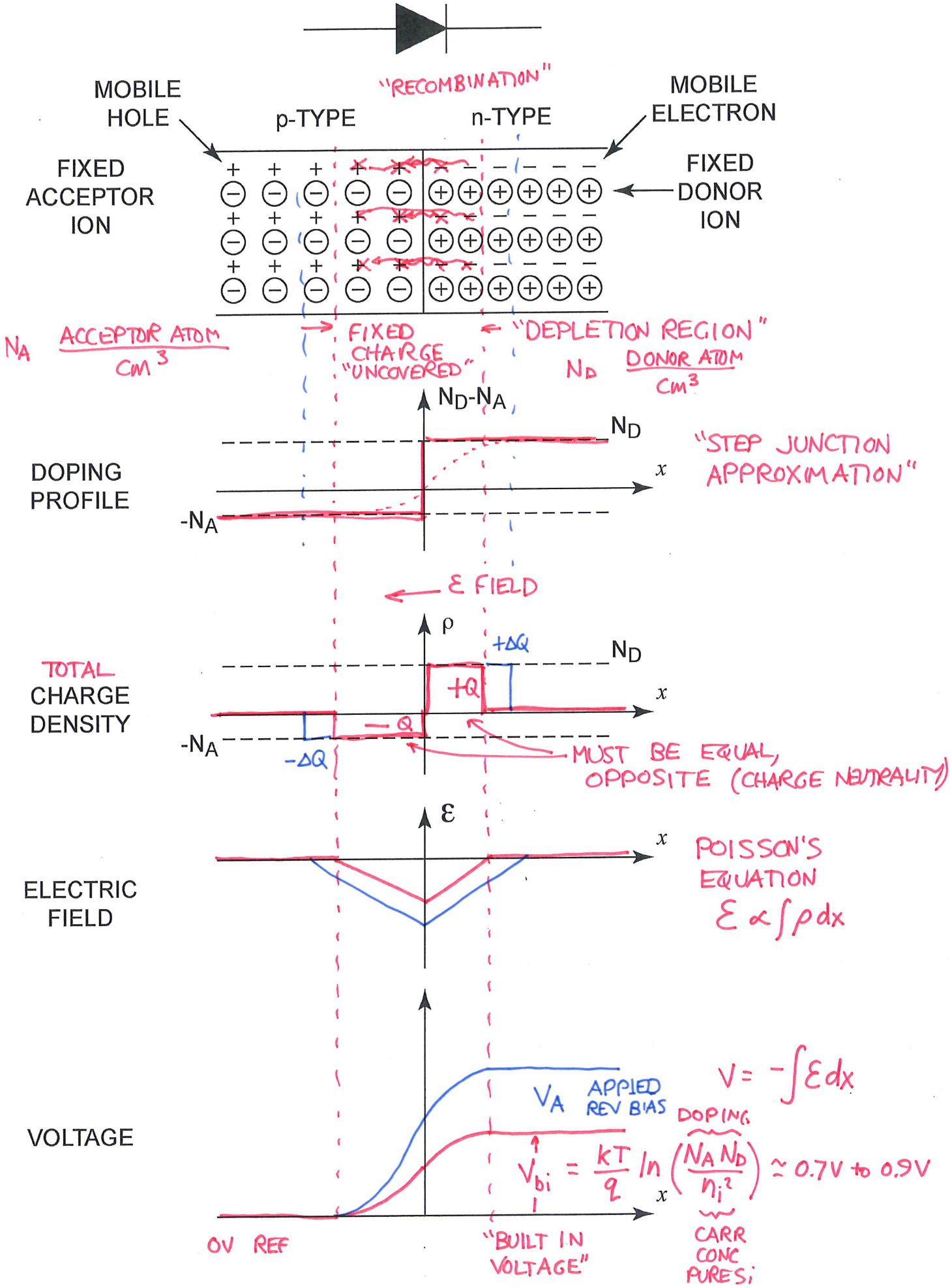


"LVS"

"TAPEOUT"

6-12 WEEKS

$100,000 → $1M+


MOBILE HOLE
"RECOMBINATION"
MOBILE ELECTRON
p-TYPE
n-TYPE
FIXED ACCEPTOR ION
FIXED DONOR ION
N_A ACCEPTOR ATOM / CM^3
FIXED CHARGE "UNCOVERED"
"DEPLETION REGION"
N_D DONOR ATOM / CM^3
DOPING PROFILE
$N_D - N_A$
N_D
$-N_A$
x
"STEP JUNCTION APPROXIMATION"
ε FIELD
TOTAL CHARGE DENSITY
ρ
$+\Delta Q$
$+Q$
$-Q$
$-\Delta Q$
MUST BE EQUAL, OPPOSITE (CHARGE NEUTRALITY)
ELECTRIC FIELD
ε
POISSON'S EQUATION
$\mathcal{E} \propto \int \rho \, dx$
VOLTAGE
$V = -\int \mathcal{E} \, dx$
V_A APPLIED REV BIAS
$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \simeq 0.7V$ to $0.9V$
DOPING
CARR CONC PURE Si
0V REF
"BUILT IN VOLTAGE"