ECE4902 Lecture 2

Finish p-n junction
- Capacitance
- Built-in voltage

E Field word association
MOSFET symbols
MOSFET "building blocks"
MOSFET channel:
- Accumulation
- Depletion
- Inversion

MOSFET Fabrication steps
Carrier Motion: Mobility
IC Passives:
Resistor
- Sheet Resistance
- "Ω per square" concept

Capacitor

Handouts:
Lecture 2 Overview
MOSFET "building blocks"
MOSFET fabrication steps
MOS process parameters
Mobility figure

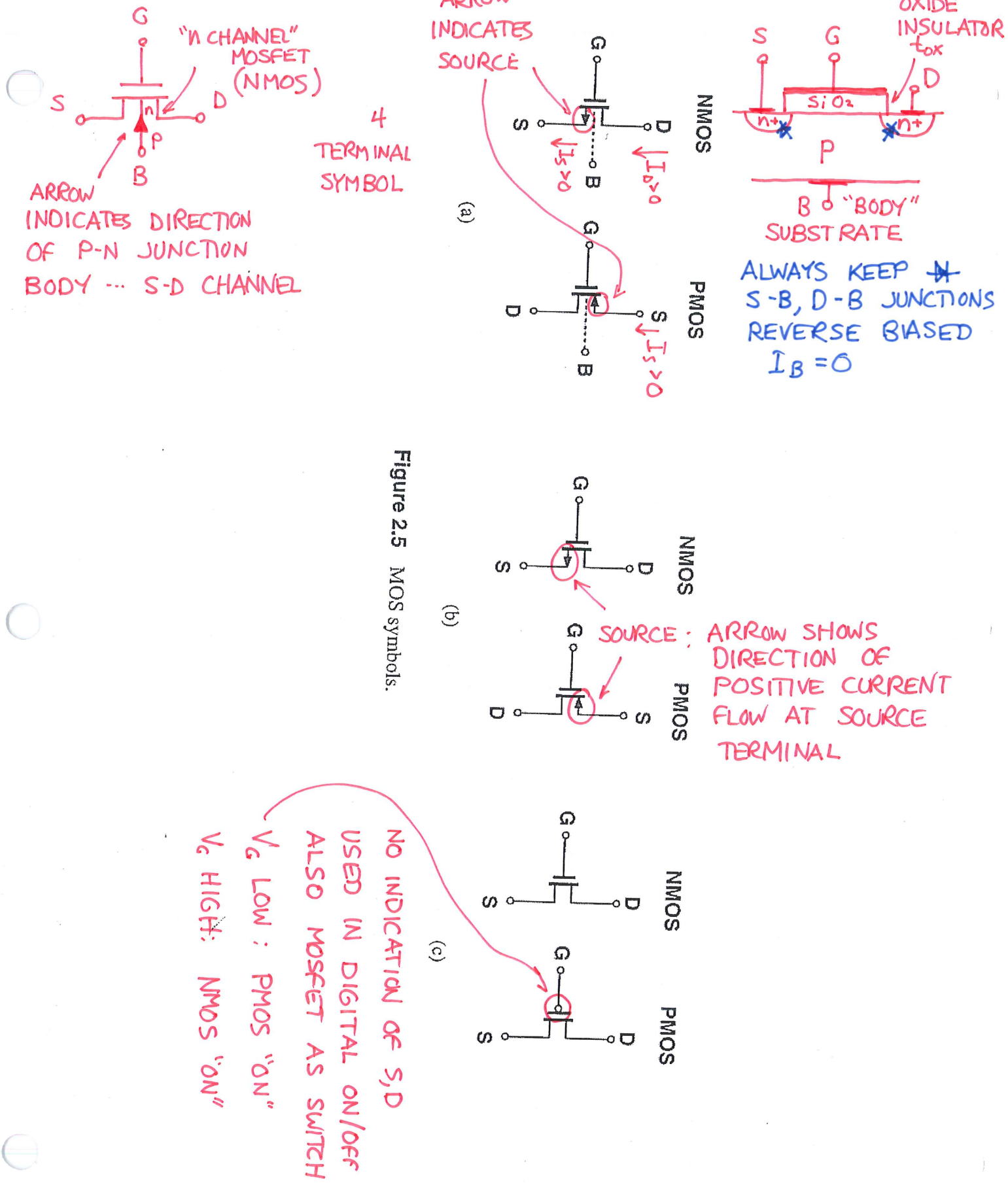
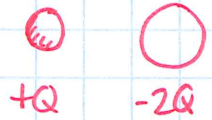
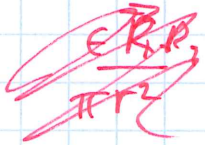


Figure 2.5 MOS symbols.

ELECTRIC FIELD

PHYSICS



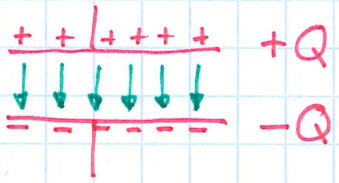


"LINES OF FORCE"

START ON + ; END ON −

KEEPS TRACK OF CHARGE CONSERVATION!

CAPACITORS



STORES CHARGE

BETWEEN PLATES

"POINTS" + TO −

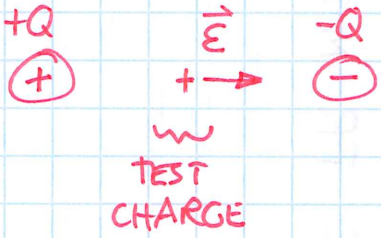
$\mathcal{E}$ FIELD IS A VECTOR

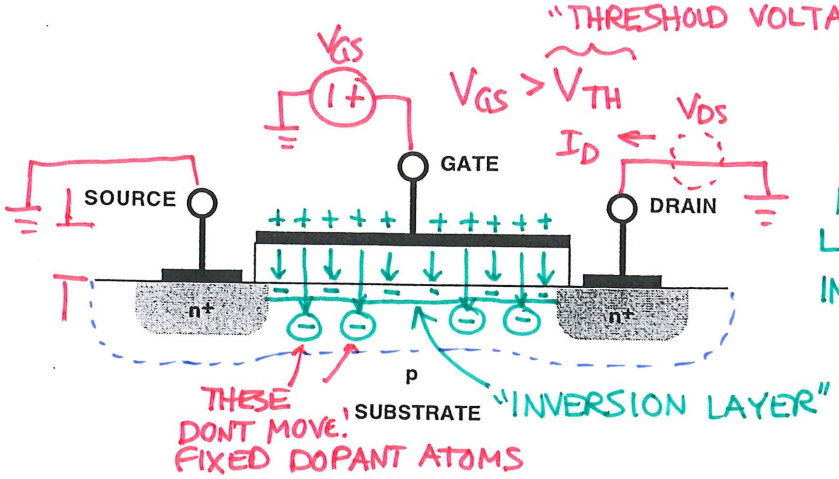
TELLS DIRECTION A + CHARGE WOULD GO

$\vec{F} = q\vec{\mathcal{E}}$

OPPOSITE Q ATTRACT

SAME Q REPEL

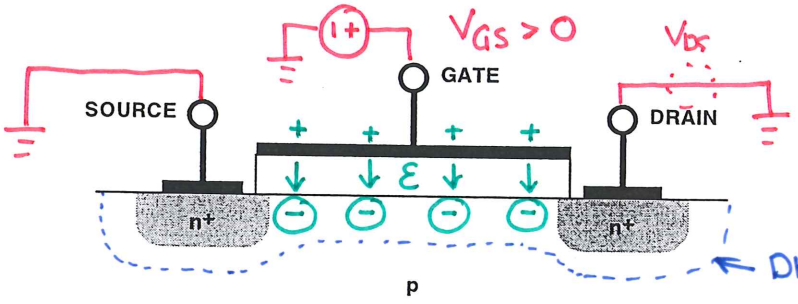




"INVERSION"

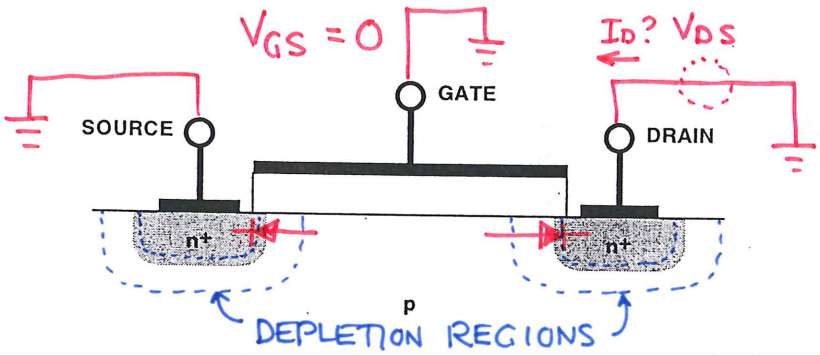
APPLY V_{DS}
$I_D > 0$ FLOWS

MORE + CHARGE ON GATE
LAYER OF MOBILE e^- ON SURFACE
INVERTED p TYPE → n TYPE
CONTINUOUS S → D

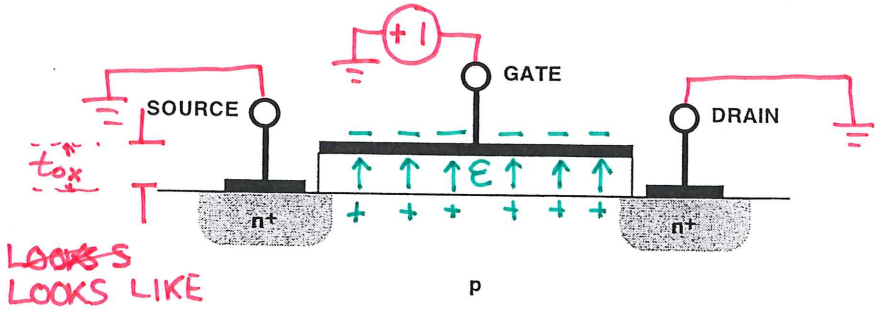


+ CHARGE ON GATE
⇒ ε FIELD INTO SUBSTRATE
⇒ HOLES PUSHED AWAY
⇒ ε FIELD LINES END ON FIXED ⊖ CHARGES "UNCOVERED"
← DEPLETION REGION EXTENDS S → D

"DEPLETION" $I_D = 0$



APPLY V_{DS}: WHAT I_D FLOWS?
S-D PATH S ○|◀|▶|○ D
BACK-TO-BACK DIODES
ONE REV BIASED
$I_D = 0$ OFF



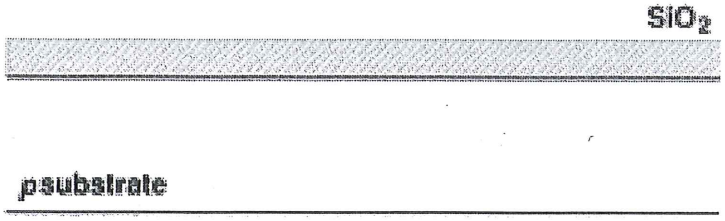
~~LOOKS~~ LOOKS LIKE PARALLEL PLATE CAPACITOR

$V_{GS} < 0$ NEGATIVE
− CHARGE ON GATE
⇒ ε FIELD

"ACCUMULATION"

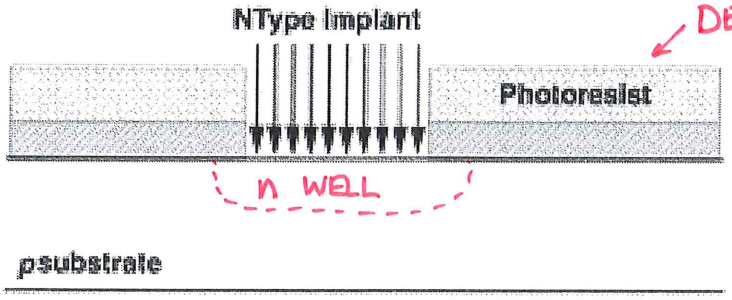
CHANNEL EVEN MORE p-TYPE $I_D = 0$

a)



← NOT GATE OXIDE
WILL DEFINE AREAS
TO BE DOPED

b)

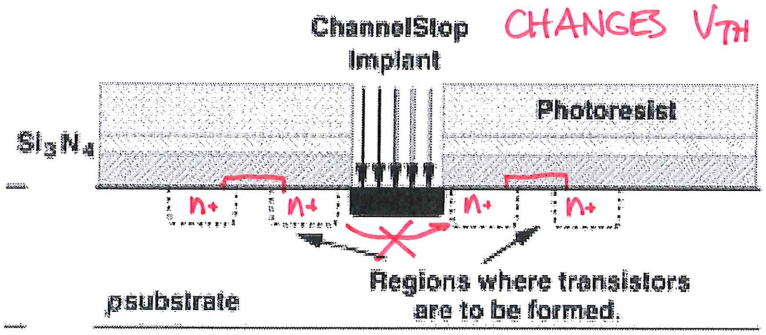


DEFINE WITH MASK

c)

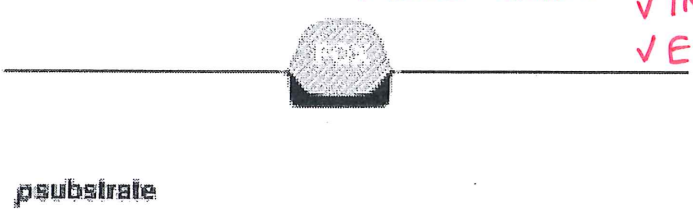
"LOCAL SUBSTRATE"
FOR PMOS DEVICES

d)



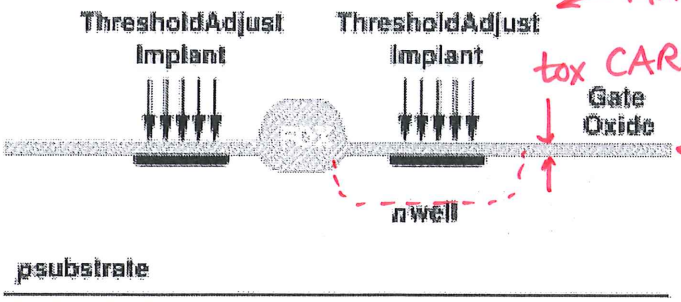
CHANGES V_{TH} FOR UNWANTED PARASITIC MOSFETS

e)



SILICON THAT WON'T BE MOSFET
FIELD OXIDE
✓ INSULATOR
✓ EFFECTIVE t_{ox} LARGE
KEEPS PARASITICS OFF

f)



← MAKES $V_{TH(P)} \approx -V_{TH(N)}$

t_{ox} CAREFULLY CONTROLLED

SAME FOR NMOS PMOS

← THIN

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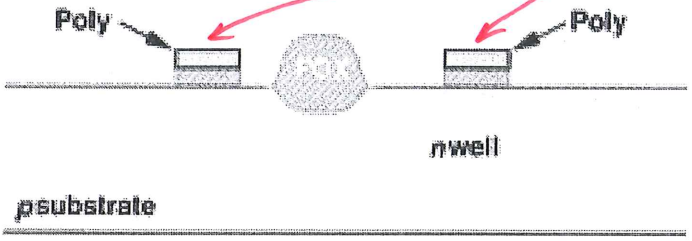
g)



GATE TERMINALS

USED AS MASK FOR S, D DIFFUSION IN FOLLOWING STEPS "SELF ALIGNED"

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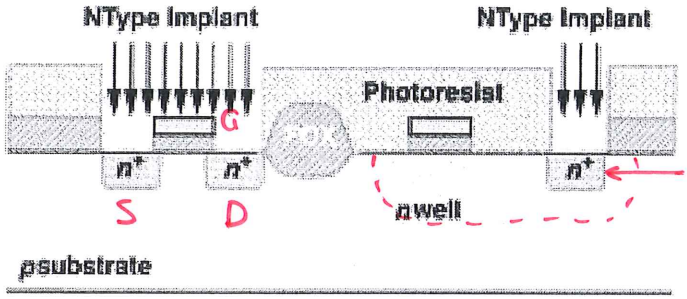
h)



← CONTACT TO nWELL OF PMOS DEVICE

NMOS

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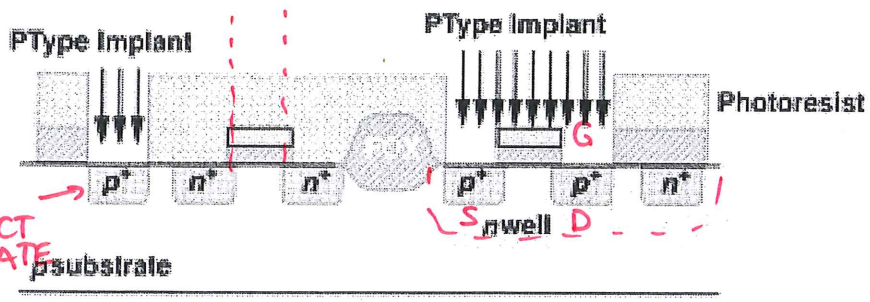
i)



PMOS

MOSIS WAFER ACCEPTANCE TESTS

SHORTEST L IN PROCESS

RUN: T6BF VENDOR: AMIS
TECHNOLOGY: SCN15 RUN TYPE: SKD FEATURE SIZE: 1.6 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SCNA16_AMIS

MOSFET GEOMETRY

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	4.0/1.6			
Vth		0.57	-0.97	volts
SHORT	20.0/1.6			
Idss		183	-72	uA/um
Vth		0.55	-0.93	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/1.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.58	-0.88	volts
Vjbkd		16.6	-14.5	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.62	0.47	V^0.5
K' (Uo*Cox/2)		35.7	-12.0	uA/V^2
Low-field Mobility		632.73	212.68	cm^2/V*s

5X W ↓

$V_{TH} \sim L, W$

"PUNCH THROUGH" BREAK DOWN GATE OXIDE (DESTRUCTIVE)

OK FOR 5V LOGIC

p-n JCT S-B, D-B

OK FOR 5V LOGIC

"OFF" LEAKAGE CURRENT

e⁻ IN NMOS

HOLES IN PMOS

$v = \mu E$

CARRIER VELOCITY $\frac{cm}{sec}$

FIELD $\frac{V}{cm}$

Each wafer fabrication run has its own code; this run is designated "T6BF"

FEATURE SIZE is the minimum gate length; 1.6µm for this process

TECHNOLOGY and RUN TYPE are more specific; these codes indicate added features in the process (for example, linear capacitors and BJTs)

Vth is the threshold voltage; MINIMUM refers to the smallest geometry devices allowed by the process design rules. For logic applications, often only minimum size devices are used.

Idss is the current per unit width with maximum voltage (in the case of this process, 5V) applied for V_{GS}. Expressing current this way allows the designer to rapidly determine required device size for a given current. For example, if 2mA of drive current is required for a P-channel MOSFET when the gate is fully turned on, the width should be
2mA / (86µA/µm) = 23.3µm
Note also that the threshold voltage Vth for the SHORT device is different than the MINIMUM case -- a second-order effect that SPICE needs to keep track of.
Vpt is the punch-through voltage, beyond which the device will be damaged.

This is the leakage current per unit width when V_{GS}=0. An important parameter for analog switch design, especially in sample-and-hold circuits when the hold capacitor can be partially discharged by the leakage current of a MOSFET which should be "off".

Again, note that the threshold voltage is affected by device geometry.
Vjbkd is the breakdown voltage of the active-substrate pn junction;
Ijlk is the reverse bias leakage current of the junction.
Gamma is the body-effect parameter, which expresses how the threshold voltage is affected by the source-substrate reverse bias voltage.

K' is the transconductance parameter used in some expressions of the square law

$$I_D = \underbrace{\frac{\mu C_{OX}}{2}}_{K'} \frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

Low-field mobility is the value of µ for E fields below the velocity saturation limited region.

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)
SCN (lambda=0.8)	0.00

"Poly bias" allows the software which writes the mask specification file to make the mask dimension larger or smaller than what is drawn in the layout software. This can account for the over- or under-etching of the polysilicon. Here "lambda" refers to the unit spatial dimension of the layout software used to design the masks (not the channel length modulation λ). See Razavi ch. 17 and Johns & Martin sec. 2.3 for more information.

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	4.8/3.2			
Vth		0.86	-1.14	volts
SHORT	9.6/3.2			
Vth		0.86	-1.09	volts
LARGE	28.8/28.			
Vth		0.87	-1.08	volts
K' (Uo*Cox/2)		21.5	-6.8	uA/V^2

In this technology, transistors can also be fabricated using a second polysilicon layer for the gate. The transistor parameters are different (and not quite as good) since the resulting MOSFETs have a thicker gate oxide.

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PARASITICS NEVER ON

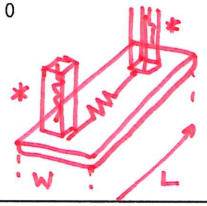
OK FOR 5V LOGIC

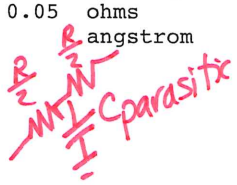
This is for a MOSFET which uses the field oxide as the gate oxide. We don't want this to function as a MOSFET (if it did, unrelated active areas could be shorted together). In this case, the field implant worked, because the threshold voltage is ~15V. Since this process is intended for 5V systems, the FOX transistor will never be on.

R

PROCESS PARAMETERS	N+	P+	POLY	POLY2	PBASE	M1	M2	UNITS
Sheet Resistance	52.2	75.6	25.0	22.3	2257.5	0.05	0.03	ohms/sq
* Contact Resistance	54.5	41.1	25.4	17.0			0.05	ohms
Gate Oxide Thickness	306							angstrom

PROCESS PARAMETERS	N_W	UNITS
Sheet Resistance	1714	ohms/sq
Contact Resistance		ohms





Contact resistance: *This is the resistance of one contact between METAL1 and the layer indicated. For example, one contact between the heavily doped N-type source or drain region of a MOSFET (N+) and the first layer of metal (M1) has a resistance of 54.5 Ω - not negligible! When it is necessary to lower resistance, many contacts are made in parallel to give a lower total resistance.*

Gate Oxide Thickness: *This is the oxide thickness tox used to determine the gate capacitance per unit area. Check by comparing to the gate oxide capacitance per unit area:*

$$\frac{\varepsilon_{OX}}{t_{OX}} = \frac{K_{OX}\varepsilon_O}{t_{OX}} = \frac{3.9(8.85E-12\ F/m)}{306E-10\ m} = 1.13E-3\ F/m^2$$

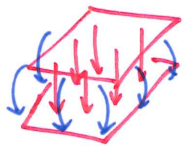
Which agrees pretty well with the 1128aF/um² for POLY-to-N+ shown below

POLY
THICK OX
SUBST
$36\ E\text{-}18\ \frac{F}{(\mu m)^2}$
PARALLEL PLATE

C

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	N_W	UNITS
Area (substrate)	291	302	36	37	21	13	129	aF/um^2
Area (N+active)			1128	730	50	26		aF/um^2
Area (P+active)			1110	723				aF/um^2
Area (poly)				592	46	23		aF/um^2
Area (poly2)					46	23		aF/um^2
Area (metal1)						38		aF/um^2
Fringe (substrate)	79	160			31	27		aF/um
Fringe (poly)					58	44		aF/um
Fringe (metal1)						55		aF/um
Overlap (N+active)			173					aF/um
Overlap (P+active)			231					aF/um

JCT CAP (ZERO BIAS)
HIGHEST (THIN OXIDE)



$C = \varepsilon \frac{A}{d}$

Sheet resistance: *These are the numbers to use when determining the physical dimensions of a resistor to achieve a certain value of resistance. The layers are:*

N+	*Heavily doped region of N-type diffusion used for source, drain of N-channel MOSFETs*
P+	*Heavily doped region of P-type diffusion used for source, drain of P-channel MOSFETs*
POLY	*Polysilicon metal used for gates of MOSFETs*
POLY2	*A second layer of polysilicon which can also be used for MOSFET gates (Also, POLY and POLY2 can be used with thin oxide between to make a linear capacitor (See capacitance parameters below)*
PBASE	*A moderately doped region of P-type diffusion used as the base for NPN bipolar transistors*
M1	*First layer of aluminum metallization; much lower sheet resistance than polysilicon or diffusion*
M2	*Second layer of metallization; lowest sheet resistance since thickness of M2 is greater than thickness of M1*
N_W	*Lightly doped region of N-type diffusion used as a well (sort of a "local substrate") used for P-channel MOSFETs*

These are parallel-plate capacitance (per unit area) between the layers indicated. For example, a capacitor using M1 and M2 as the plates will have a capacitance of 38aF/μm² (atto is 1E-18) per micron squared. A capacitor 100μm x 100μm has an area of 1E+4μm², so the capacitance would be 380E-15 F, or 0.38pF.

Fringe and overlap capacitances are edge effects, and therefore are given per unit length. The 100um x 100um capacitor mentioned in the example above would have a perimeter of 400um. The fringe capacitance from M1 to M2 is 55aF/μm. Thus the capacitance due to the fringing field would be (400μm)(55aF/μm)=22 E-15 F = 22fF. Total for the 100um x 100um capacitor will be the sum of contributions from parallel plate + fringing: 0.38pF + 22fF = 0.402pF.