ECE4902 Lecture 5

Small Signal Model Development
- Transconductance g_m
  - Design Tradeoffs
- Channel Length Modulation
- Body Effect

Transconductance g_m Expressions

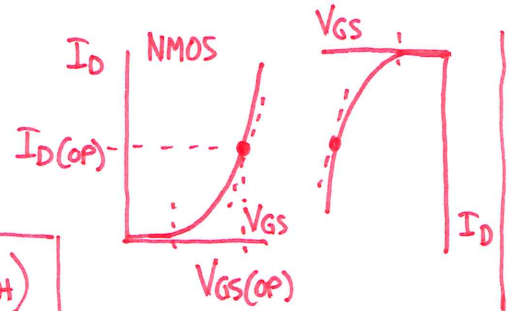
Common Source Amplifier
- Example: Small signal gain, CD4007 parameters
- How to Increase Gain?

Hand In:
HW 2

Handout:
Lecture Overview
Small Signal Model Development
Transconductance g_m Expressions
Channel Length Modulation
Common Source Amplifier (Again)

DEFINITION:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{\text{OP POINT}}$$



$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$$

(OVERDRIVE)

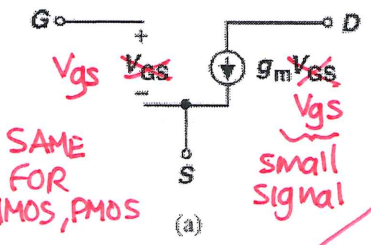
$$g_m = \frac{2I_D}{(V_{GS}-V_{TH})}$$

$$g_m = \sqrt{2I_D\,\mu C_{ox}\frac{W}{L}}$$

g_m TRANSCONDUCTANCE

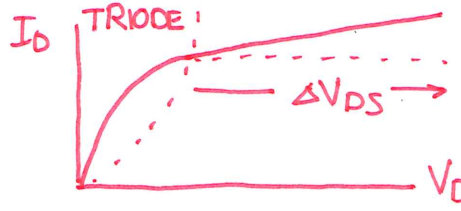
$V_G \rightarrow I_D$ $\quad \frac{\Delta I}{\Delta V}$

SAME FOR NMOS, PMOS



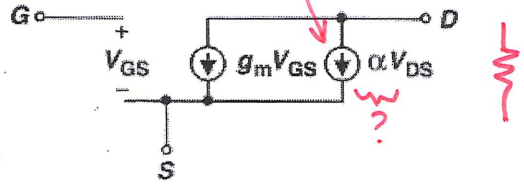
V_{gs} small signal

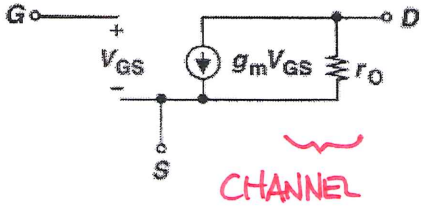
CHANGING V_{DS} ALSO AFFECTS I_D!?



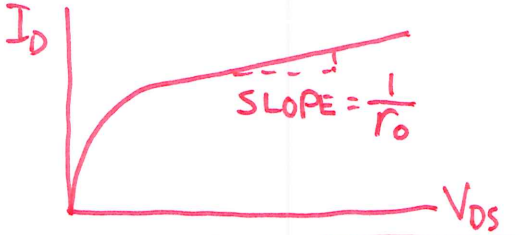
$\frac{\Delta I_D}{\Delta V_{DS}}$ BOTH AT DRAIN!

DEPENDENT SOURCE





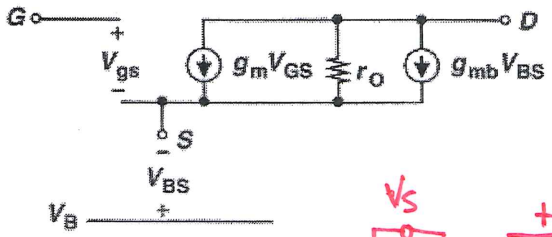
CHANNEL LENGTH MODULATION IN small signal model



$$r_O = \frac{1}{\frac{dI_D}{dV_{DS}}}$$

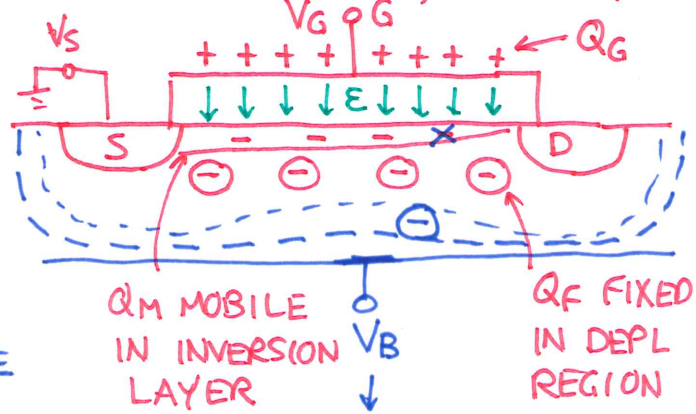
DEFINITION

$$r_O = \frac{1}{\lambda I_D}$$



"BODY EFFECT"

LOOK AT CHANNEL, MOBILE Q



WHAT IF $V_B \neq V_S$?

SUPPOSE $V_B \downarrow$

$\Rightarrow$ SIZE OF DEPLETION REGION INCREASES $\Rightarrow$ MORE FIXED CHARGE "UNCOVERED" $\Rightarrow Q_F \uparrow \Rightarrow Q_M \downarrow \Rightarrow I_D \downarrow$

MODEL AS INCREASE IN V_{TH}

$$\frac{\Delta I_D}{\Delta V_B} = g_{mb}$$

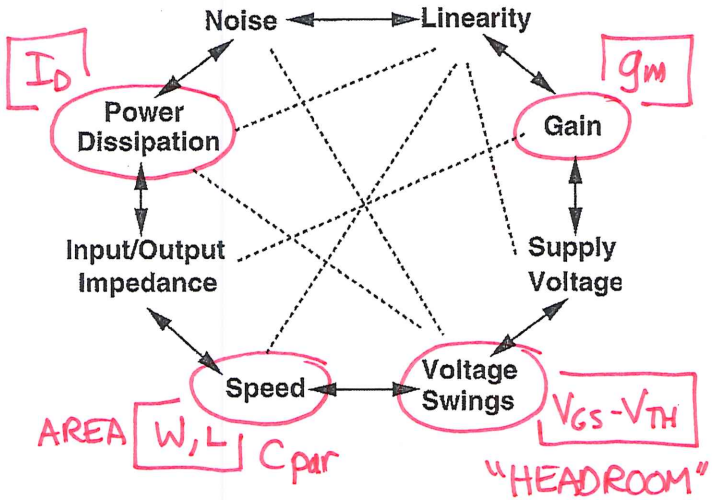
$\Rightarrow$ COMMON SOURCE: $V_S = V_B \Rightarrow g_{mb} = 0$

$\frac{dI_D}{dV_{GS}}$

g_m EXPRESSIONS

	CONSTRAINT	WHAT TO DO TO INCREASE g_m?	LARGE SIGNAL "SIDE EFFECT"
$\frac{2I_D}{(V_{GS}-V_{TH})}$	I_D (FIXED POWER)	⇒ REDUCE $(V_{GS}-V_{TH})$	$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2$ ($\frac{W}{L}$ ⇑ AREA COST; $(V_{GS}-V_{TH})$ ↓)
$\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$	$V_{GS}-V_{TH}$ (VOLTAGE "HEADROOM")	⇒ INCREASE $\frac{W}{L}$ (MIN)	I_D ↑ POWER COST
$\sqrt{2I_D\,\mu_n C_{ox}\frac{W}{L}}$	W, L FIXED AREA (PARASITIC CAP Cpar)	⇒ INCREASE I_D	$(V_{GS}-V_{TH})$ MUST ↑ HEADROOM COST

Figure 3.2 Analog design octagon.



"g_m EFFICENCY"

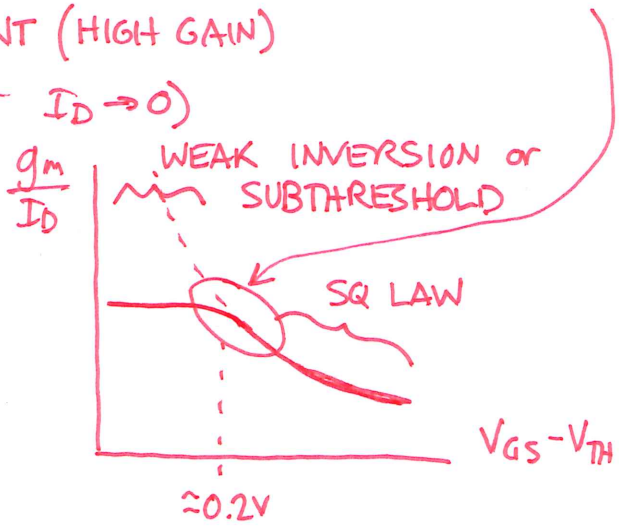
$\frac{g_m}{I_D}$ } WHAT WE WANT (HIGH GAIN)

$\frac{g_m}{I_D}$ } SPEND (WANT $I_D \to 0$)

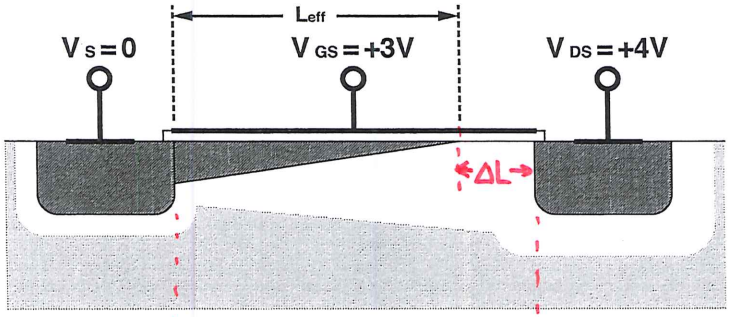
WANT THIS HIGH

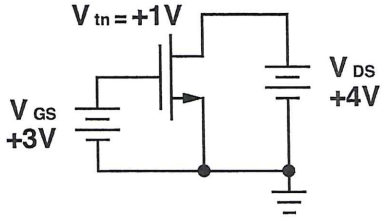
$\frac{2I_D}{V_{GS}-V_{TH}}\frac{1}{I_D} = \frac{2}{V_{GS}-V_{TH}}$

USUALLY START WITH $V_{GS}-V_{TH} \simeq 0.2$ TO 0.3 V



ECE4902 Physical Significance of Channel Length Modulation Parameter λ





SQUARE LAW WITH CHARGE DISTRIBUTION LENGTH

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L_{eff}}(V_{GS}-V_{TH})^2$$

$L_{eff} = L - \Delta L$

L: MASK (GEOMETRY)

ΔL: ELECTRICAL EFFECT CAUSED BY CHANGE IN V_{DS}

WRITE L_{eff} AS $L_{eff} = L\left(1 - \frac{\Delta L}{L}\right)$ FRACTIONAL CHANGE CAUSED BY ΔV_{DS}

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L\left(1-\frac{\Delta L}{L}\right)}(V_{GS}-V_{TH})^2$$

USE $\frac{1}{1-\varepsilon} \approx 1+\varepsilon$

WITH THIS APPROX

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2\left(1+\frac{\Delta L}{L}\frac{\Delta V_{DS}}{\Delta V_{DS}}\right)$$

$\frac{\Delta L}{L}\frac{\Delta V_{DS}}{\Delta V_{DS}} = \lambda$

CHANNEL LENGTH MODULATION PARAMETER

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2\left[1+\lambda V_{DS}\right]$$

$[1+\lambda V_{DS}]$ CAPTURES CHANNEL LENGTH MOD

UNITS: $\frac{1}{V}$ V^{-1}

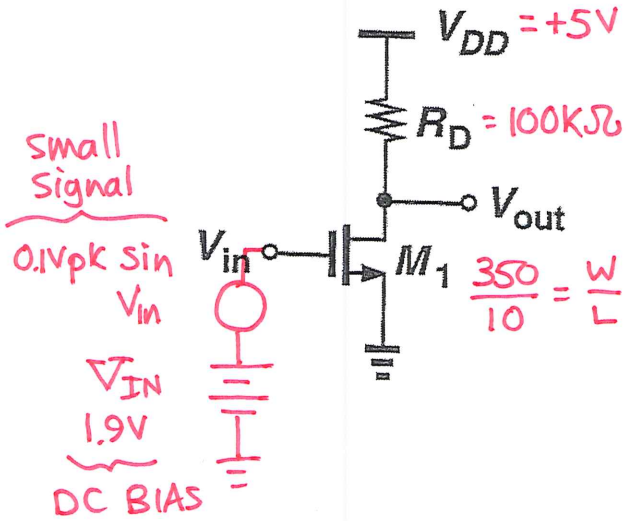
$\lambda = \frac{1}{L}\frac{\Delta L}{\Delta V_{DS}}$ } CHANGE IN EFFECTIVE LENGTH } CAUSED BY CHANGE IN V_{DS}

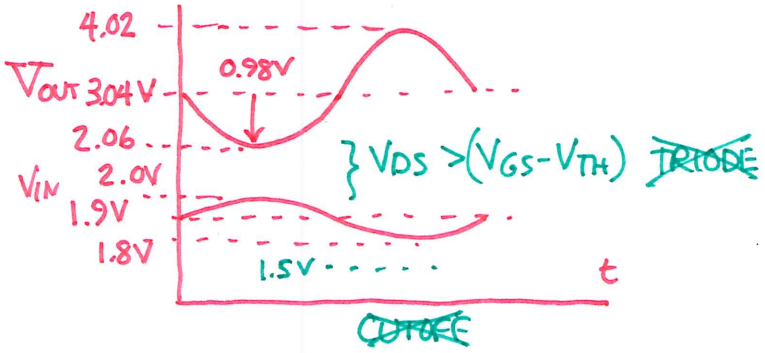
W AS A FRACTION OF OVERALL LENGTH

IDEAL: $\lambda = 0$

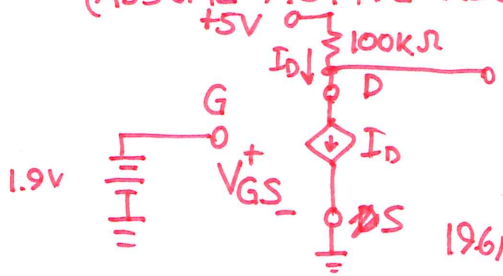
small signal model for common source amplifier with resistive load

Sec. 3.2 Common-Source Stage





DC BIAS: LARGE SIGNAL MODEL
(ASSUME ACTIVE REGION; CHECK!) ACTIVE ✓

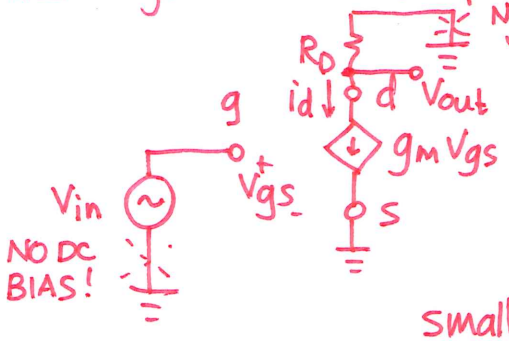


$V_{OUT} = +5V - I_D(100K\Omega)$ — SQ LAW

$19.6\mu A = \frac{7.0E\text{-}6}{2}\frac{350}{10}(1.9V - 1.5V)^2$ — 0.4V OVERDRIVE

$V_{OUT} = +5V - \underbrace{(19.6\mu A)(100K\Omega)}_{1.96\,V} = 3.04V$

Small signal model (simplest)



$V_{out} = -id\,R_D = -g_m V_{in} R_D$

$id = g_m V_{gs}$, $V_{gs} = V_{in}$

$g_m = \frac{2I_D}{(V_{GS}-V_{TH})} = \frac{2(19.6\mu A)}{0.4V} = 98\,\frac{\mu A}{V}$

OPERATING POINT LARGE SIGNAL QUANTITIES

small signal gain

$\frac{V_{out}}{V_{in}} = -g_m R_D$

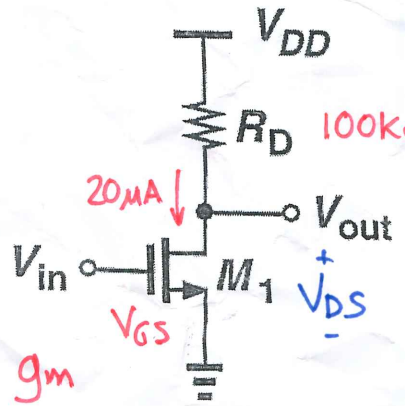
$= -(9.8E\text{-}5)(100K\Omega)$

$= -9.8$

180° ϕ INVERSION

Example process parameters		NMOS	PMOS	Units
Threshold voltage	V_t	+1.50	-1.50	V
Mobility- C_{ox} product	μC_{ox}	7.0 E-6	2.5 E-6	A/V^2
Channel length modulation	λ	0.03	0.05	V^{-1}

HOW TO MAKE $\left|\frac{V_{out}}{V_{in}}\right|$ BIGGER?



GAIN: $|g_m R_D|$

WAS ≈ 10

$\left|\frac{V_{out}}{V_{in}}\right| = g_m R_D$

↑ ↑

10X 10X

$g_m(1M\Omega) = 100$ ✓

INCREASE VALUE OF R_D!

SAME I_D (V_{GS} DIDN'T CHANGE)

⇒ SAME g_m

STILL IN ACTIVE REGION?

LARGE SIGNAL: $V_{OUT} = V_{DS} = V_{DD} - I_D R_D$ (TOO BIG)

$= 5V - \underbrace{20\mu A \; 1M\Omega}_{20V}$

$= 5V - 20V = -15V$

TRIODE CRASH!

FIX: REDUCE I_D

WHAT I_D? MAXIMIZE SIGNAL SWING WITH V_{OUT} OPERATING POINT $\frac{V_{DD}}{2} = 2.5V$

$\frac{2.5V}{1M\Omega} = 2.5\mu A$ FIXES LARGE SIGNAL PROBLEM

⇒ WILL REDUCE g_m! $\frac{2(2.5\mu A)}{0.4V} = 12\frac{\mu A}{V}$

CHANGED $\frac{W}{L}$

$g_m R_D \approx 12$!

INCREASE g_m!

$g_m = \frac{2I_D}{(V_{GS}-V_{TH})}$ } INCREASE I_D ⇒ TRIODE CRASH!

REDUCE R_D

OUTPUT DC BIAS: $V_{OUT} \approx \frac{V_{DD}}{2} = I_D R_D$ } LARGE SIGNAL

small signal gain

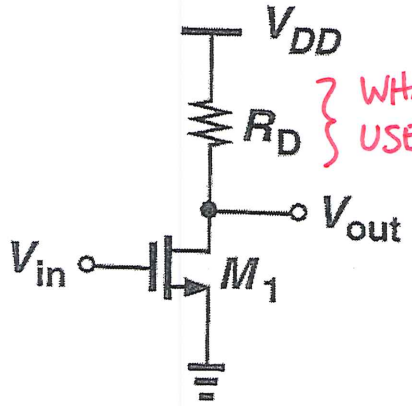
$$\underbrace{g_m R_D}_{\frac{2 I_D}{(V_{GS}-V_{TH})}} \Rightarrow \left|\frac{V_{out}}{V_{in}}\right| = \frac{2 I_D R_D}{(V_{GS}-V_{TH})} \Rightarrow \frac{\cancel{2}\,\frac{V_{DD}}{\cancel{2}}}{(V_{GS}-V_{TH})} = \frac{V_{DD}}{(V_{GS}-V_{TH})}$$

V_{DD}: FIXED 5V

$(V_{GS}-V_{TH})$: $\geq 0.2V$ (SUBTHR)

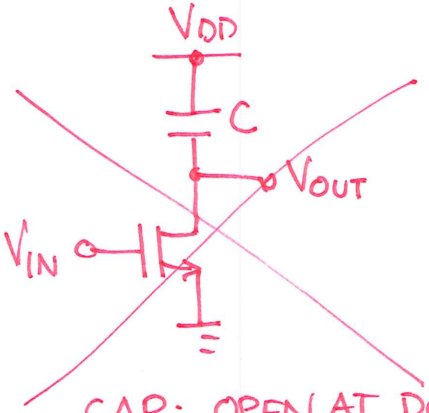
25 BEST EVER

Sec. 3.2 Common-Source Stage



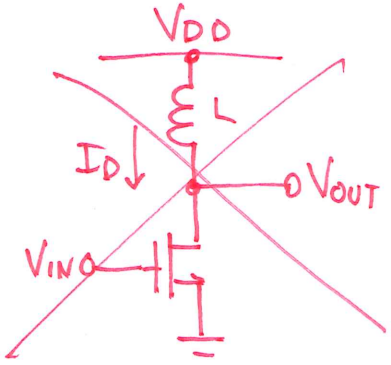
WHAT ELSE COULD WE USE HERE INSTEAD OF RESISTOR?

CAPACITOR?



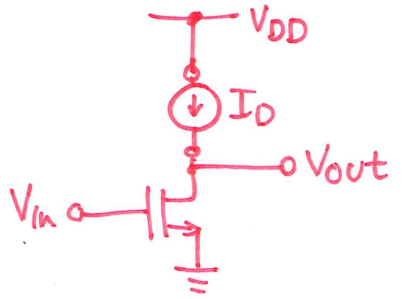
CAP: OPEN AT DC
NO PATH FOR I_D
$I_D = 0$ $g_m = 0$

INDUCTOR?



DC PATH ✓
$Z_L = 0$ AT DC
ZERO DC GAIN
(OK FOR RF)
~~OP-AMP~~

WANT $g_m R_D$ HIGH
INCREASE R_D

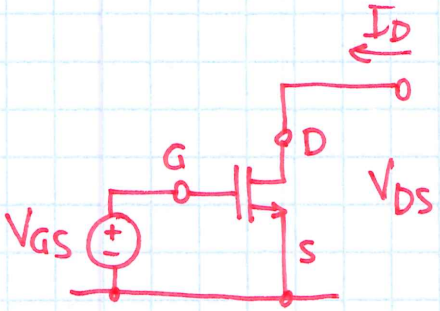


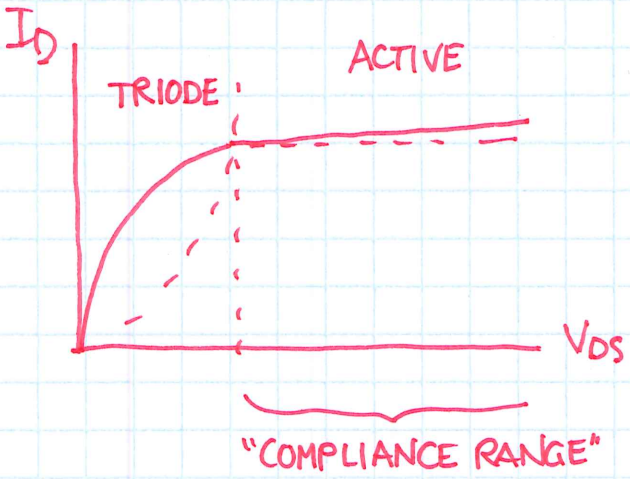
WHAT IS HIGHEST RESISTANCE
$R_D = \infty$
OPEN CIRCUIT!
NOT SO GOOD FOR DC BIAS

CURRENT SOURCE;
OPEN SMALL signal model
ALLOWS DC CURRENT IN
LARGE SIGNAL

HOW TO IMPLEMENT CURRENT SOURCE?

MOSFET WITH CONSTANT V_{GS}





SQUARE LAW FOR CHOOSING V_{GS}

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

μC_{ox}: $\propto T^{-2.3}$

$T \uparrow 10\%$

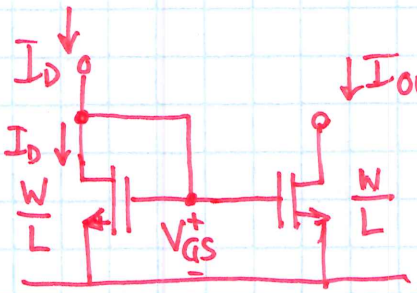
$\mu \downarrow 23\%$

$V_{GS} - V_{TH}$: TEMPCO $\approx -2 \frac{mV}{°C}$

CHANGE V_{GS} "THE OTHER WAY"

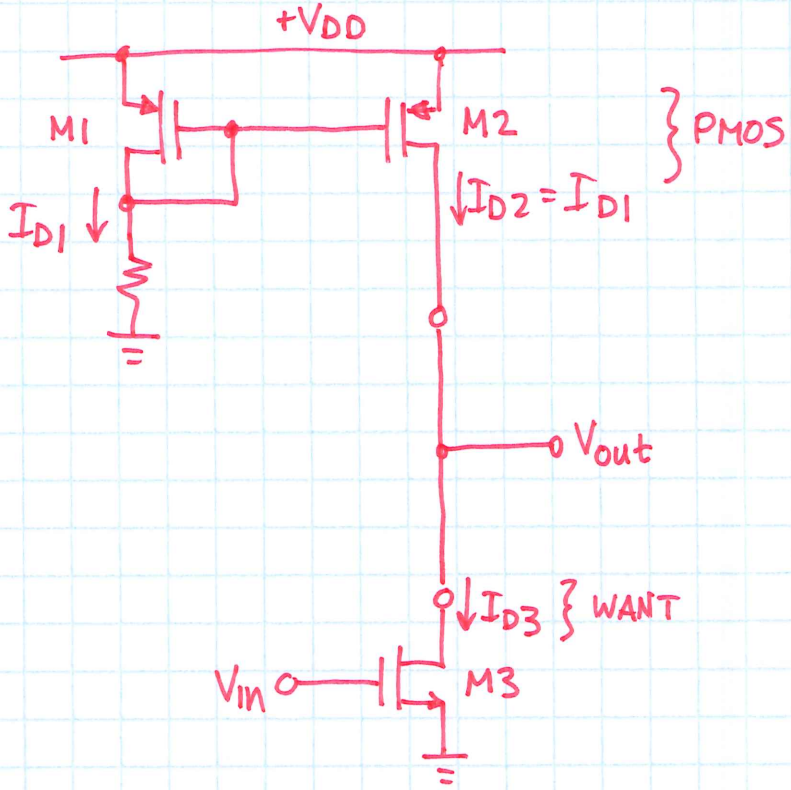
50% CHANGE I_D $0°C \rightarrow 50°C$

"DIODE CONNECTED MOSFET"



BOTH IN ACTIVE REGION

"CURRENT MIRROR"



COMMON SOURCE AMPLIFIER WITH ACTIVE LOAD

CURRENT MIRROR