ECE4902 Lecture 7

Common Source with Active Load
Design Example

Bandwidth (6.2)
Miller Effect

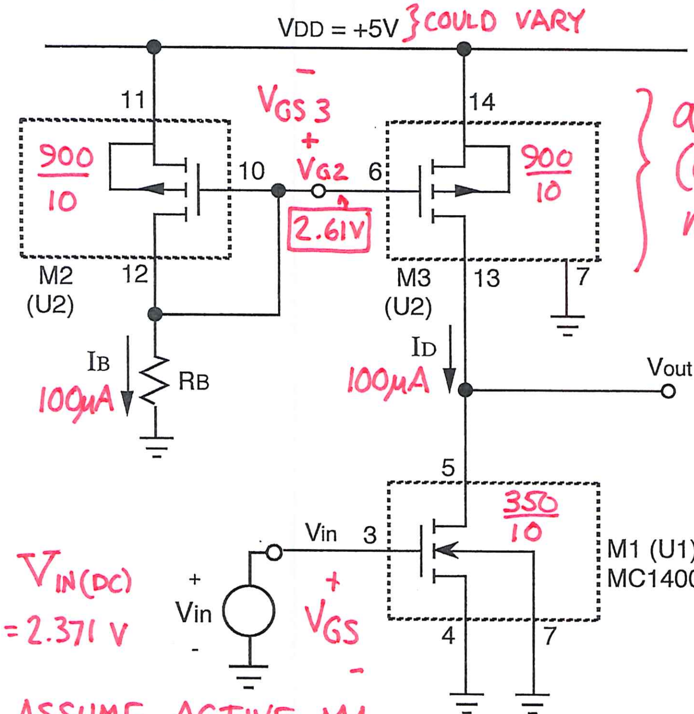
Differential Pair

Hand In:
HW 3

Handouts:
Design Example
Transfer Function: Poles & Nodes
Miller Effect
3 Cases of Differential Pair
Bartlett's Bisection Theorem
Lab 7 Differential Pair Circuits

Design example: common source amplifier with active load

Determine input DC bias and value of R_B required for V_{OUT} DC bias of 2.5V and DC drain current of 100μA



active load (current mirror)

$V_{OUT(DC)} = 2.5V$

common source amplifier

$V_{IN(DC)} = 2.371\ V$

ASSUME ACTIVE M1 SQUARE LAW

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2\left[1+\lambda V_{DS}\right]$$

$$100\mu A = \frac{7E\text{-}6}{2}\,\frac{350}{10}\,(V_{GS}-1.5V)^2\left[1+\underbrace{(0.03)(2.5V)}_{0.075}\right]$$

$$V_{GS} = \underbrace{\sqrt{\frac{100\mu A}{1.075}\,\frac{2}{7E\text{-}6}\,\frac{10}{350}}}_{\pm 0.871} + 1.5V = 2.371$$

+NMOS
−PMOS

± 0.871 } $V_{GS}-V_{TH} < V_{DS} = 2.5V$

✓ACTIVE

FOR M3: ASSUME ACTIVE SQ LAW

$$100\mu A = \frac{2.5E\text{-}6}{2}\,\frac{900}{10}\,(V_{GS3}+1.5V)^2\left[1+\underbrace{(0.05)(2.5)}_{0.125}\right]$$

$$V_{GS3} = -1.5V + \underbrace{\sqrt{\frac{100\mu A}{1.125}\,\frac{2}{2.5E\text{-}6}\,\frac{10}{900}}}_{\pm 0.89V}$$

$\pm 0.89V$ CHOOSE − FOR PMOS

$$V_{GS3} = -1.5V - 0.89V = -2.39V$$

KVL TO GATES OF MIRROR:

$$V_{DD} + V_{GS3} = V_{G2} = 5V + (-2.39V) = 2.61V$$

$V_{DS2} \neq V_{DS3}$ $\quad I_{D2}, I_{D3}$ A LITTLE DIFFERENT (CHANNEL LENGTH MOD)

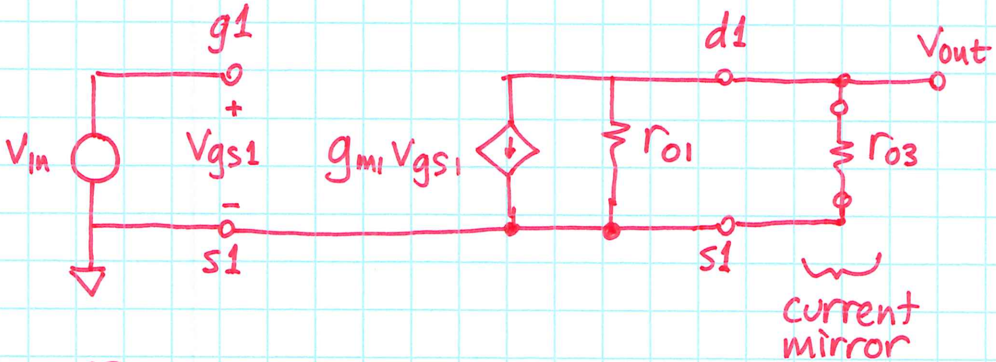
IGNORE FOR NOW: $I_{D2} = I_{D3} = 100\mu A$

$$R_B = \frac{2.61V}{100\mu A} = 26.1\ k\Omega$$

DISADVANTAGE: I_B SENSITIVE TO V_{DD} CHANGE (SOLVE WITH BIAS BLOCK, BANDGAP V REF)

Example process parameters		NMOS	PMOS	Units
Threshold voltage	V_t	+1.50	-1.50	V
Mobility- C_{ox} product	μC_{ox}	7.0 E-6	2.5 E-6	A/V^2
Channel length modulation	λ	0.03	0.05	V^{-1}

small signal gain



$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{TH1})} = \frac{2(100\mu A)}{0.871} = 230\mu A/V$$

$$r_{o1} = \frac{1}{\lambda_1 I_{D1}} = \frac{1}{(0.03)(100\mu A)} \quad 330k\Omega$$

$$r_{o3} = \frac{1}{\lambda_3 I_{D3}} = \frac{1}{(0.05)(100\mu A)} = 200k\Omega$$

$$R_{out} = r_{o1} \| r_{o3} = 125k\Omega$$

$$\frac{V_{out}}{V_{in}} = -g_{m1}R_{out} = -\left(\frac{230\mu A}{V}\right)(125k\Omega) = \underbrace{-29}_{\text{LARGE } V_{GS}-V_{TH}} \Rightarrow -120$$

FIX: SMALLER $(V_{GS}-V_{TH}) \Rightarrow 0.22$

$$\frac{2}{(\lambda_1+\lambda_3)(V_{GS}-V_{TH})}$$

Transfer function: Poles associated with circuit nodes

Cascade of noninteracting blocks

$$\frac{V_{out}}{V_{in}} = \left(\frac{V_{out}}{V_2}\right)\left(\frac{V_2}{V_1}\right)\left(\frac{V_1}{V_{in}}\right)$$

PRODUCT OF INDIVIDUAL BLOCK TRANSFER FUNCTIONS! (1)

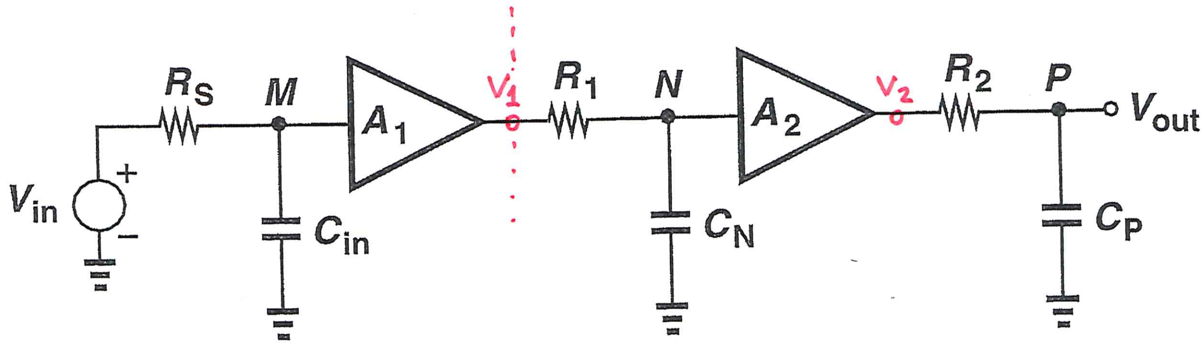


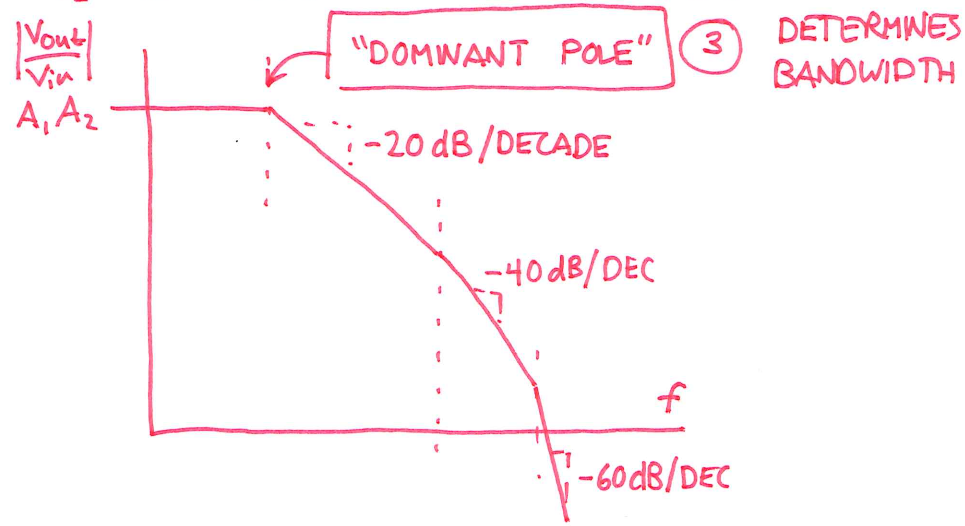
Figure 6.6 Cascade of amplifiers.

$$\frac{V_1}{V_{in}} = \left(\frac{1}{1+sR_SC_{in}}\right)A_1 \qquad \frac{V_2}{V_1} = \left(\frac{1}{1+sR_1C_N}\right)A_2 \qquad \frac{V_{out}}{V_2} = \frac{1}{1+sR_2C_P}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_1A_2}{\underbrace{(1+sR_SC_{in})(1+sR_1C_N)(1+sR_2C_P)}}$$

EACH POLE OF $\frac{V_{out}}{V_{in}}$ TRANSFER FUNCTION (2)

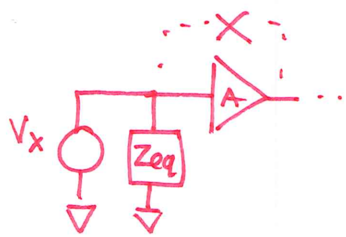
ASSOCIATED WITH NODE IN THE PHYSICAL CIRCUIT

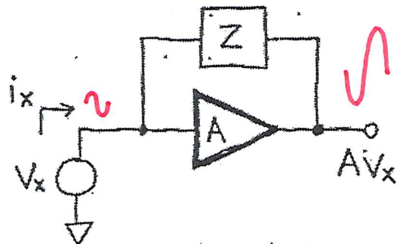


Miller effect

EE4902 MILLER EFFECT

Consider any amplifier (not necessarily an op-amp) with gain A, and some impedance Z from input to output: what impedance does it "look like"?





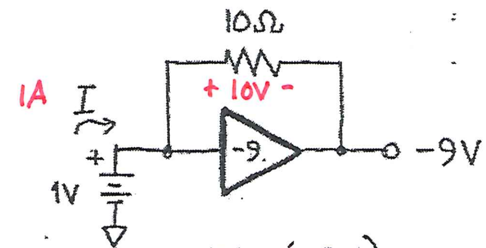
$$i_x = \frac{V_x - AV_x}{Z}$$

$$\boxed{\frac{V_x}{i_x} = \frac{Z}{(1-A)}}$$

Impedance is reduced by factor (1-A)

EXAMPLE: $Z = 10\Omega$ resistor

$A = -9$; $V_x = 1V$



$$I = \frac{1V - (-9V)}{10\Omega} = 1A$$

Applying 1V causes 1A to flow: source "sees" a 1Ω resistor!

$1\Omega = 10\Omega / (1 - [-9])$

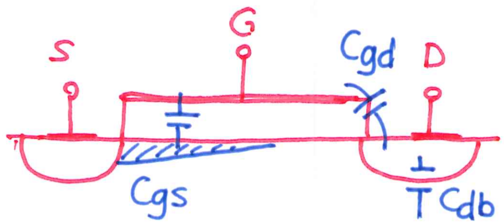
WHEN Z IS A CAPACITANCE: $Z = \frac{1}{j\omega C}$

$$\frac{V_x}{i_x} = \frac{1}{j\omega \underbrace{(1-A)C}}$$

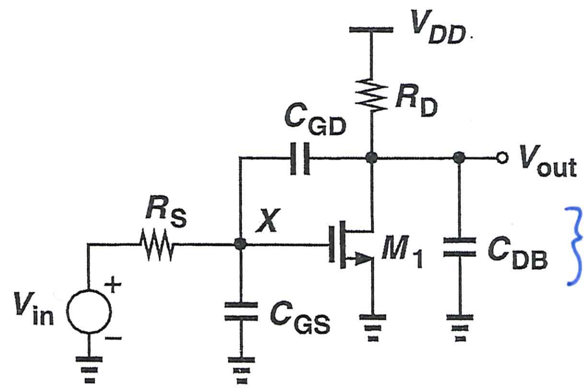
APPARENT VALUE OF C MULTIPLIED BY (1-A)!

LARGE INCREASE WHEN A IS INVERTING GAIN

Miller effect in common source stage



PARASITICS



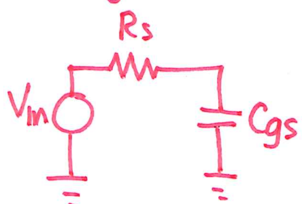
} ANY C_L WILL ADD IN PARALLEL

Figure 6.10 High-frequency model of a common-source stage.

IF C_{DB} DOMINATES

$$BW = \frac{1}{2\pi R_D C_{DB}}$$

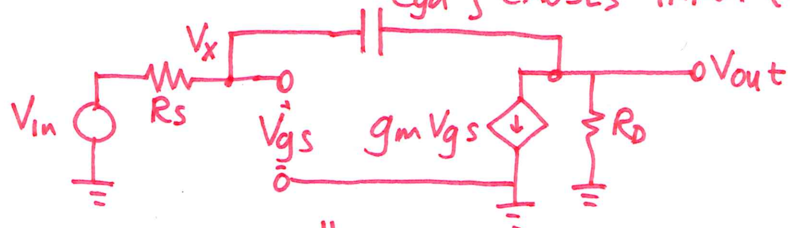
IF C_{gs} DOMINATES



$$BW = \frac{1}{2\pi R_s C_{gs}}$$

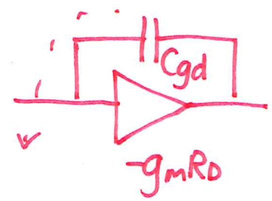
SMALL SIGNAL MODEL

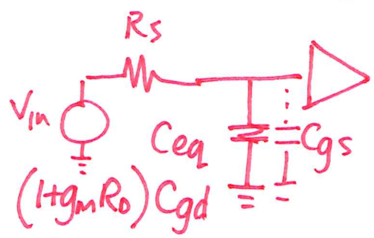
Cgd } CAUSES INPUT (V_x) ⟷ OUTPUT (V_{out}) INTERACTION



⇒ CAN'T USE SIMPLE CASCADED STAGES MODEL !?

⇓ MILLER EFFECT

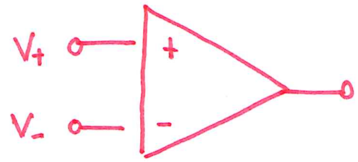




$$BW = \frac{1}{2\pi R_s[(1+g_m R_D C_{gd})+C_{gs}]}$$

Differential pair motivation:

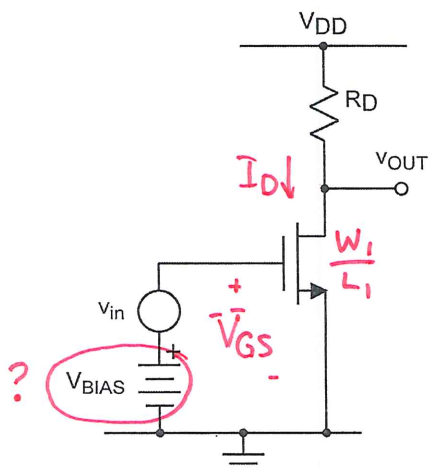
1) Op-amp input



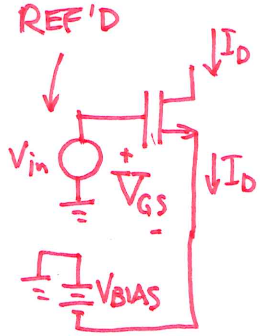
SINGLE-ENDED OUTPUT

$$V_{out} = A\underbrace{(V_+ - V_-)}_{\text{DIFFERENCE OF 2 VOLTAGES}}$$

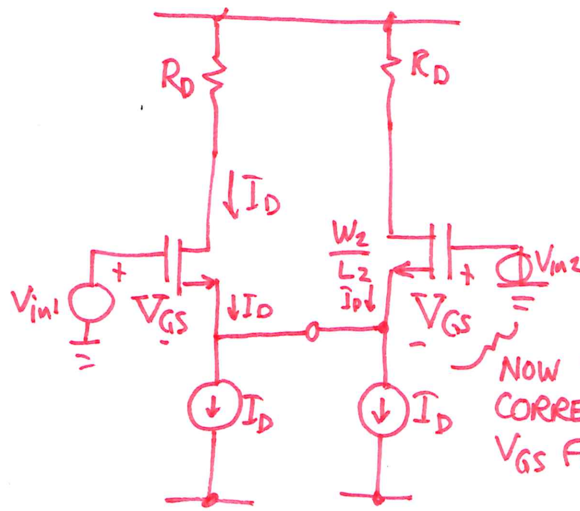
2) DC bias of common source amplifier



NICE: V_{in} GROUND REF'D

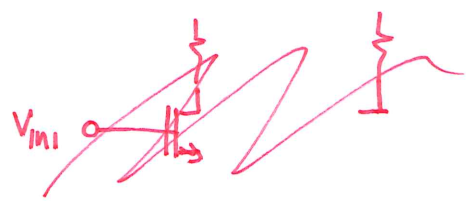


FORCE ANOTHER MOSFET TO CARRY I_D

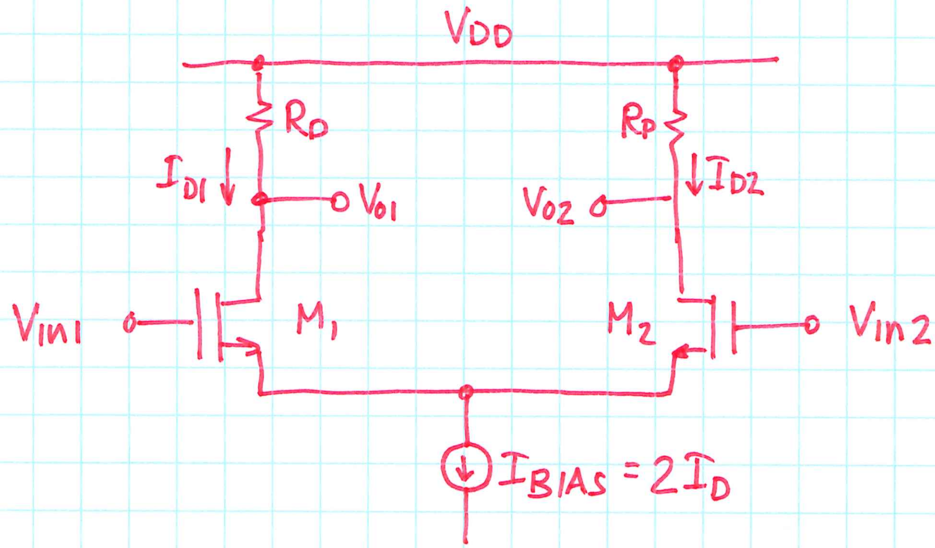


$\frac{W_2}{L_2} = \frac{W_1}{L_1}$

NOW THE CORRECT V_{GS} FOR I_D



DIFFERENTIAL PAIR



} GROUND REF'D INPUTS

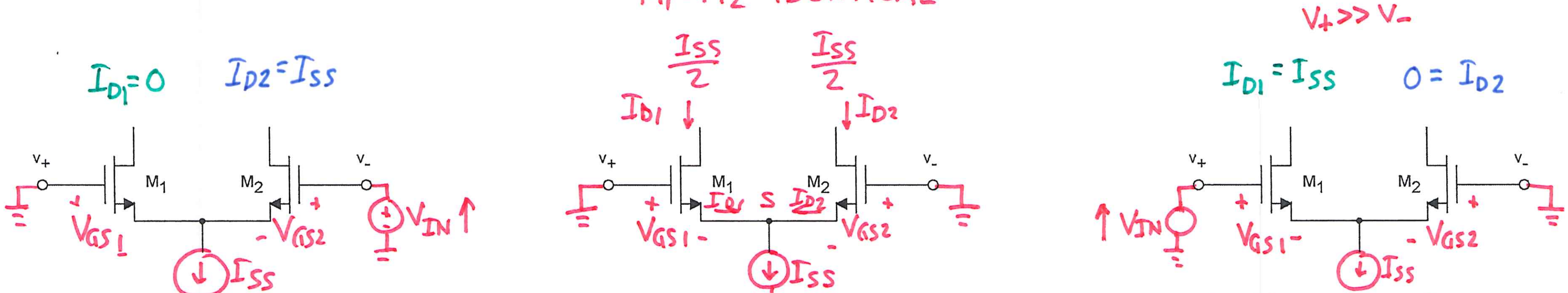
} BIAS WITH CURRENT SOURCE (MIRROR)

OUTPUT VOLTAGES:

$$V_{o1} = V_{DD} - I_{D1} R_D \qquad V_{o2} = V_{DD} - I_{D2} R_D$$

Building up differential amplifier characteristic

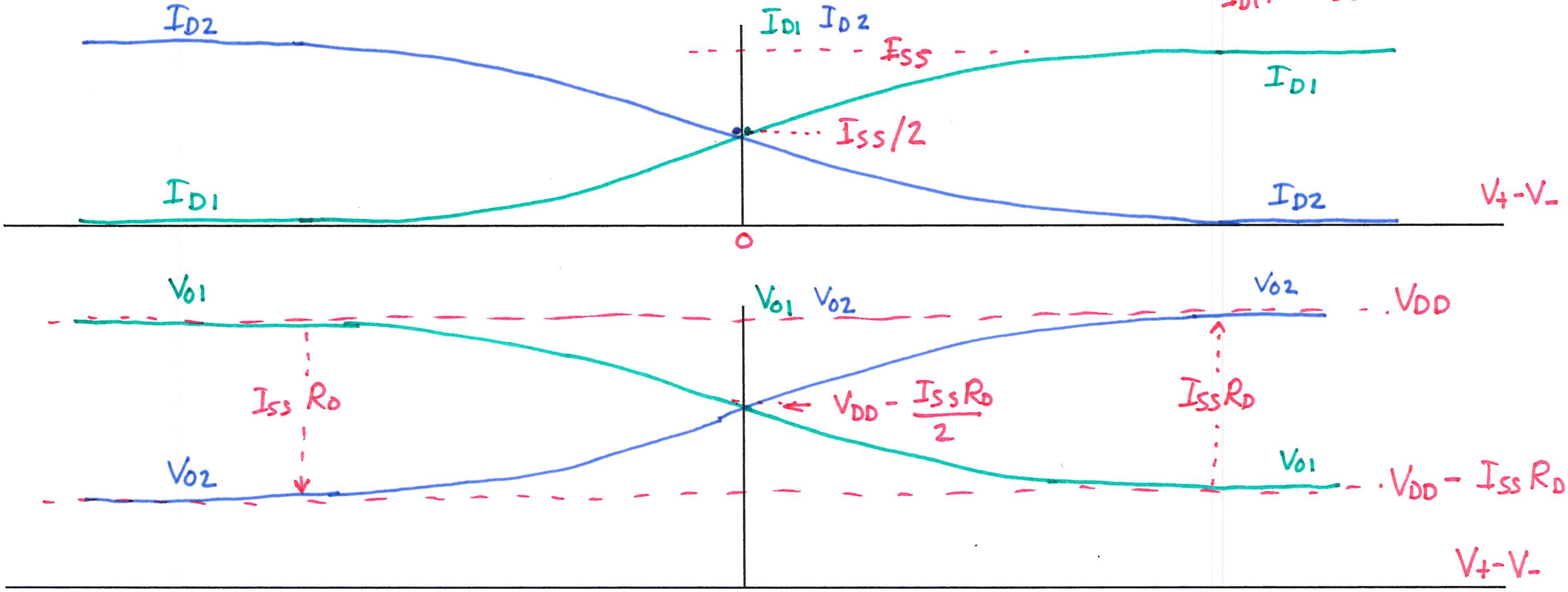
ASSUME DRAIN VOLTAGES V_{D1}, V_{D2} OK FOR ACTIVE REGION
$M_1 = M_2$ IDENTICAL



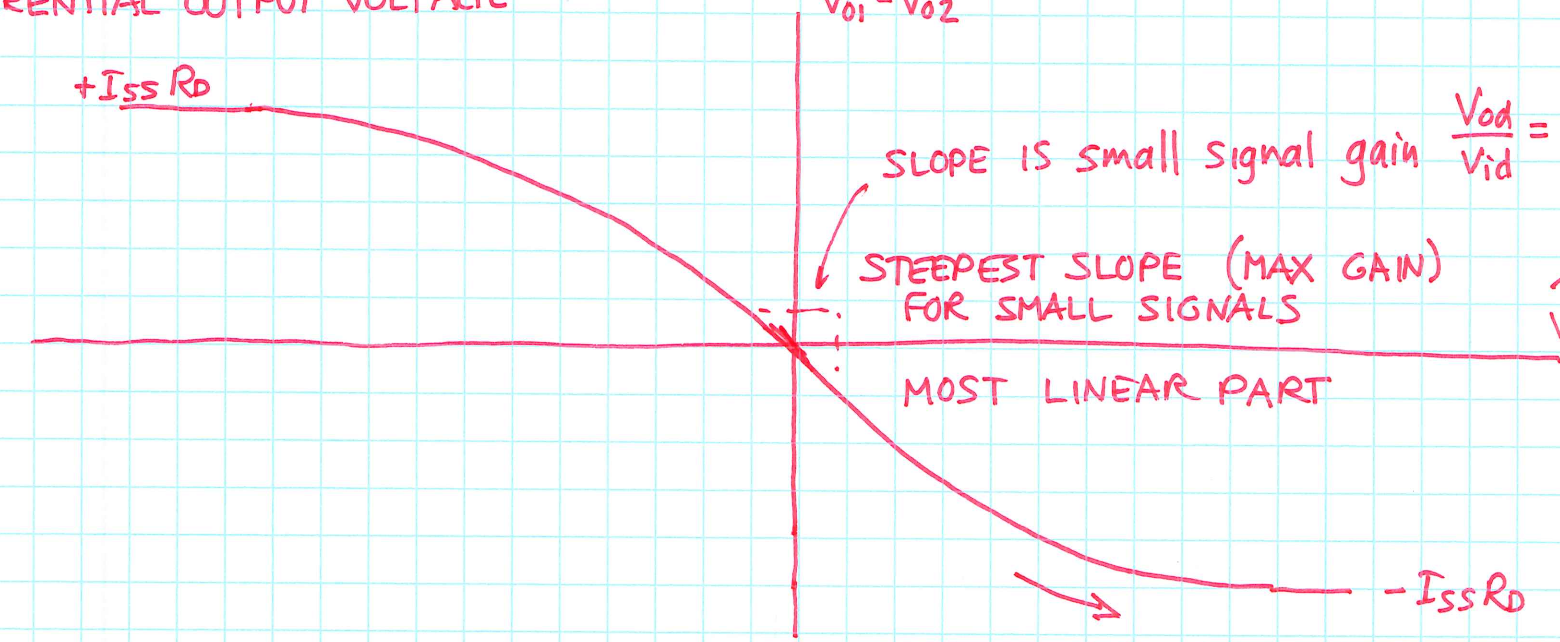
$V_{GS2} > V_{GS1}$
$I_{D2} > I_{D1}$

CONNECTION: $V_{GS1} = V_{GS2}$
$\Rightarrow I_{D1} = I_{D2}$
KCL @ S: $I_{D1} + I_{D2} = I_{SS}$

KVL: $V_{IN} - V_{GS1} + V_{GS2} = 0$
$V_{IN} = V_{GS1} - V_{GS2}$
$\uparrow \quad I_{D1} \uparrow \quad I_{D2} \downarrow$



DIFFERENTIAL OUTPUT VOLTAGE



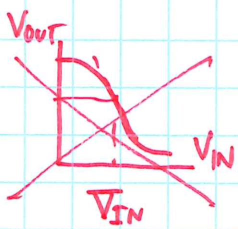
SLOPE IS small signal gain $\frac{V_{od}}{V_{id}} = -g_m R_D$ ★

STEEPEST SLOPE (MAX GAIN)
FOR SMALL SIGNALS

MOST LINEAR PART

SOFT, SYMMETRIC
CLIPPING

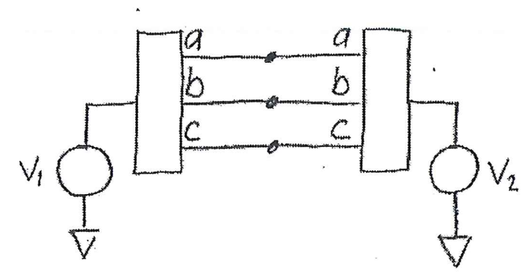
ZERO $\underbrace{\text{IN}}_{V_+ - V_-}$ → ZERO $\underbrace{\text{OUT}}_{V_{o1} - V_{o2}}$



BARTLETT'S BISECTION THEOREM

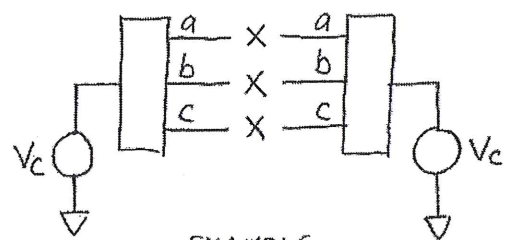
Analysis using symmetry – "half circuit"

Consider two completely symmetrical circuits: a, b, c are connected points of symmetry



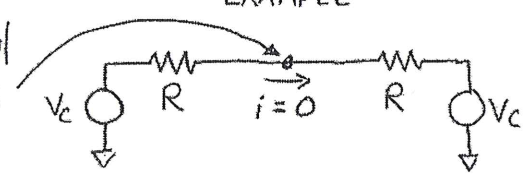
COMMON MODE

If $V_1 = V_2 = V_c$ (both circuits have the same input; symmetric excitation) ⇒ then we can open all leads between points of symmetry without affecting circuit operation; no current flows across any connection



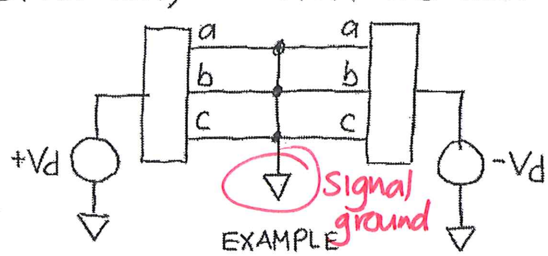
EXAMPLE: $i = 0$ (no voltage drop across Rs due to symmetrical excitation. We can open this connection without affecting performance

EXAMPLE



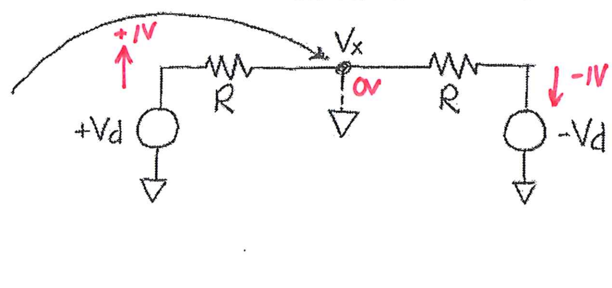
DIFFERENTIAL MODE

If $V_1 = -V_2$ (antisymmetric excitation) ⇒ then we can signal ground all leads between points of symmetry



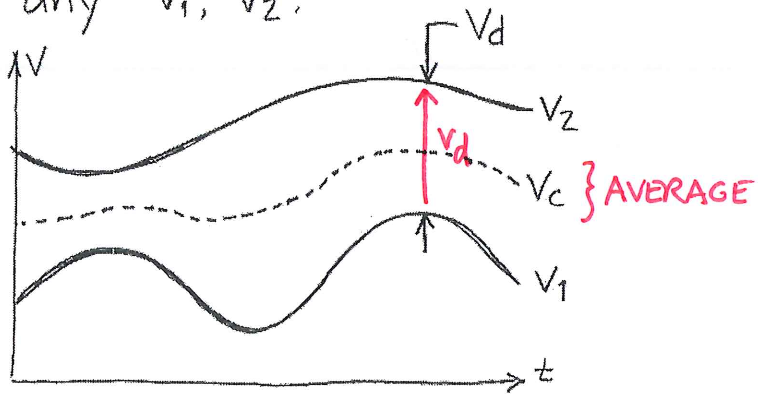
EXAMPLE: by voltage divider, $V_x = 0$ regardless of V_d. Therefore we can signal ground this connection without affecting circuit performance

EXAMPLE



Any two signals can be expressed in terms of common mode, differential mode

Consider any V_1, V_2:



Define

$$V_c = \frac{V_1 + V_2}{2}$$

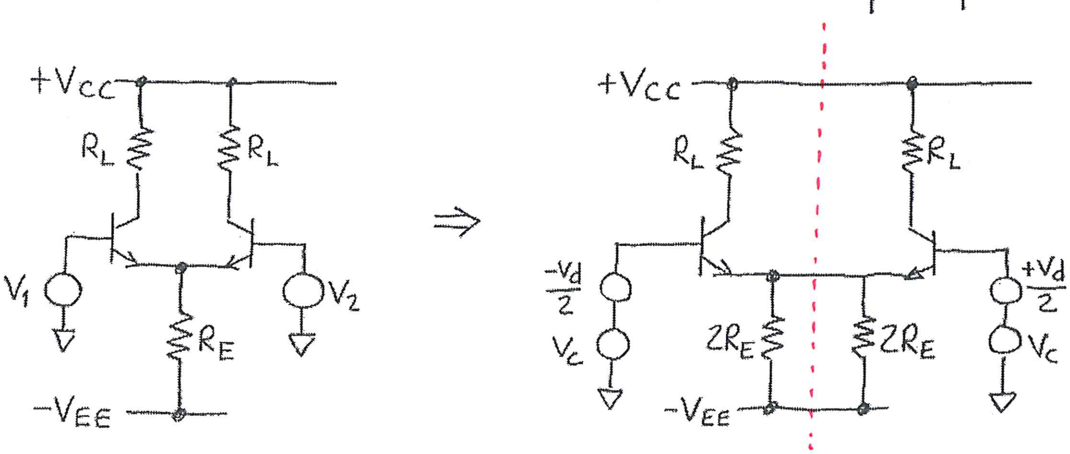
$$V_d = V_2 - V_1$$

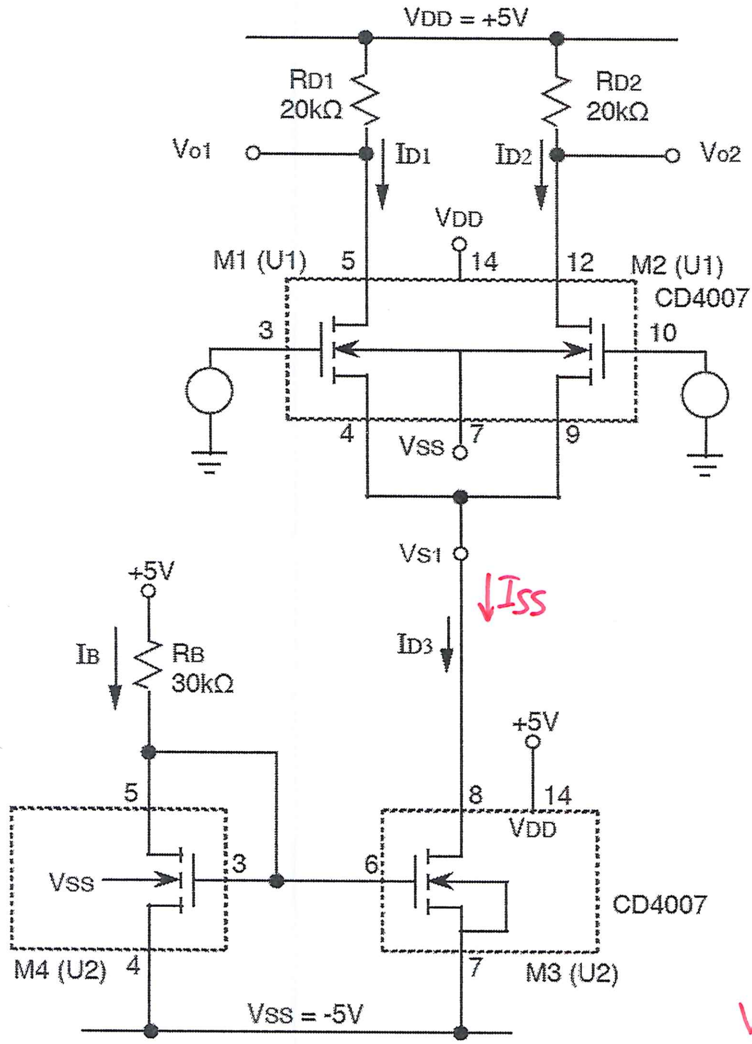
Straightforward to verify that

$$V_1 = V_c - \frac{V_d}{2}$$

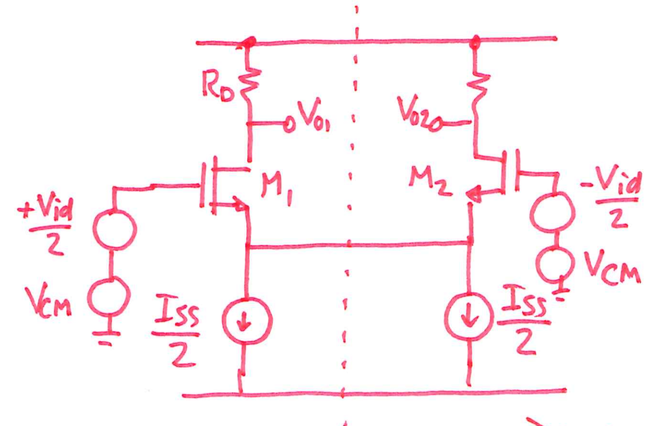
$$V_2 = V_c + \frac{V_d}{2}$$

Key: analyze differential amplifier by decomposing inputs into v_c and v_d, then using symmetry (Bartlett's bisection theorem) and superposition

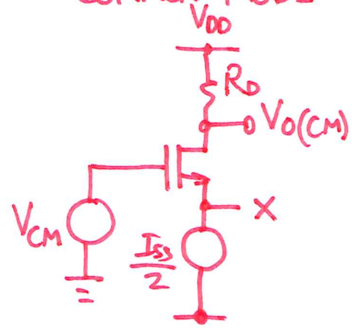




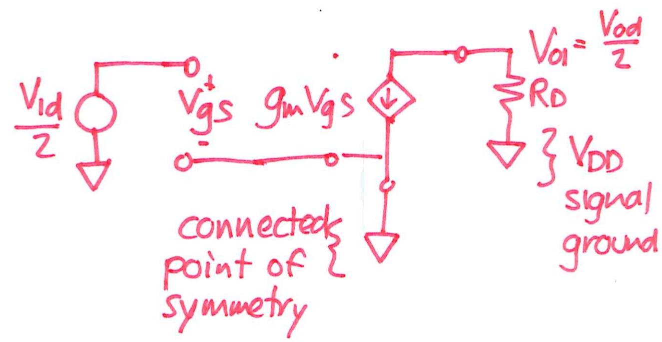
REDRAW FOR SPLIT



COMMON MODE



DIFFERENTIAL MODE (small signal)



DC BIAS:

$I_{D1} = \frac{I_{SS}}{2}$

$V_{O(CM)} = V_{DD} - \frac{I_{SS} R_D}{2}$

$\frac{V_{od}/2}{V_{id}/2} = -g_{m1} R_D$ } same as CS amplifier

☆