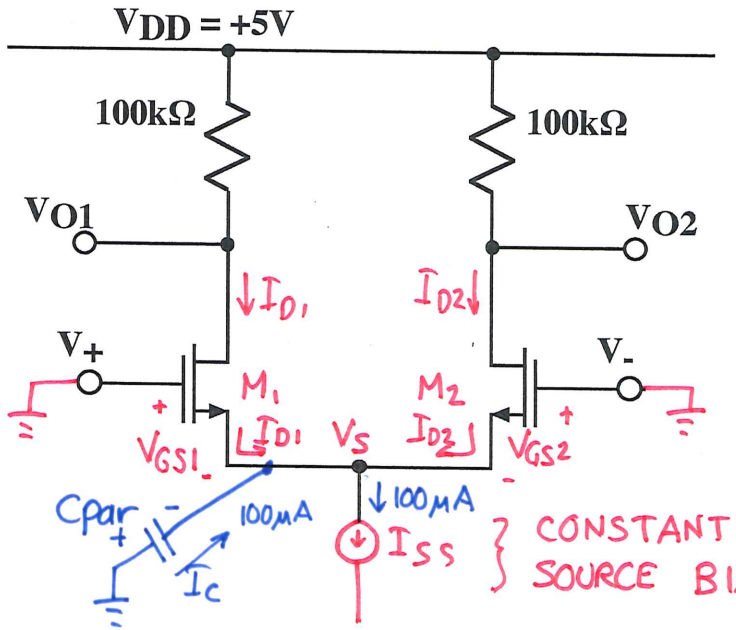
ECE4902 Lecture 8

Differential Pair
- Current Source Bias
- Analysis Example
- Diff Pair with Active Load

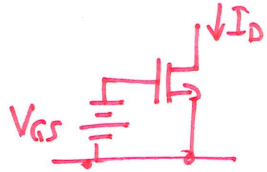
2-Stage Op-Amp

Online: HW 4
(due *December 1*!
Happy Thanksgiving!)

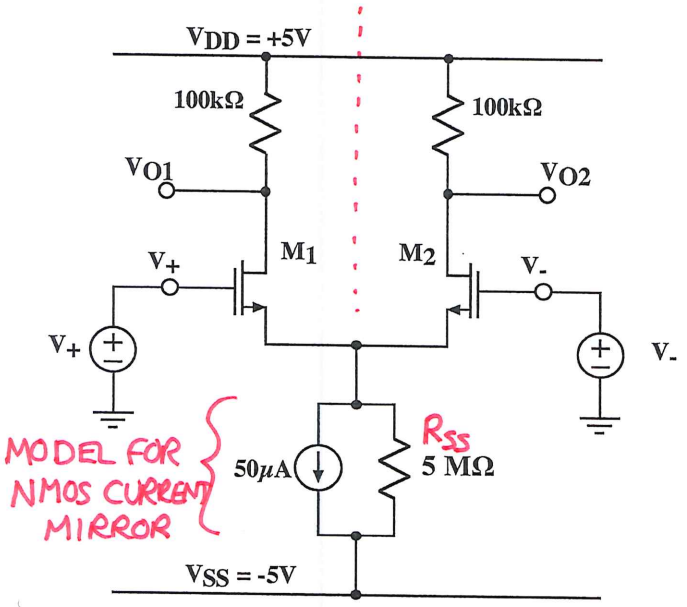
Handout:
Lecture 8 Topics
Analysis Example
Active Load Development
2-Stage Op-Amp Development
Lab 8/9 Op-amp



COMMON SOURCE: NEED TO SET V_{GS} BIAS "JUST RIGHT"



DIFF PAIR: HOW DO WE KNOW
I_{SS}, V_S WILL CAUSE CORRECT V_{GS1}, V_{GS2}
FOR $I_{D1} + I_{D2} = I_{SS}$?
SUPPOSE $V_S = 0$ (WRONG! $V_{GS} = 0 \rightarrow I_{D1}, I_{D2} = 0$)
100 μA WILL FLOW IN Cpar PARASITIC CAP
Cpar WILL CHARGE + TO - SO V_S ↓
V_{GS1}, V_{GS2} WILL INCREASE: I_{D1}, I_{D2} INCREASE
EQUILIBRIUM WHEN $I_C = 0 \Rightarrow I_{D1} + I_{D2} = I_{SS}$ ✓
→ INHERENTLY SETS V_S FOR CORRECT V_{GS}



- Find the DC operating point for the circuit (device currents and DC node voltages) ✓
- Draw the half-circuit representations for the common mode and differential mode circuits.
- Determine the common mode and differential mode gains
- Sketch the total output waveforms V_{O1} and V_{O2} for a purely differential input of a 10mV peak sine wave.
- Sketch the total output waveforms V_{O1} and V_{O2} for a common mode input of a 1V peak sine wave.

For M1, M2: $\frac{\mu C_{ox}}{2}\frac{W}{L} = 3.0E-4\frac{A}{V^2}$

$V_{TH} \approx 1V$?

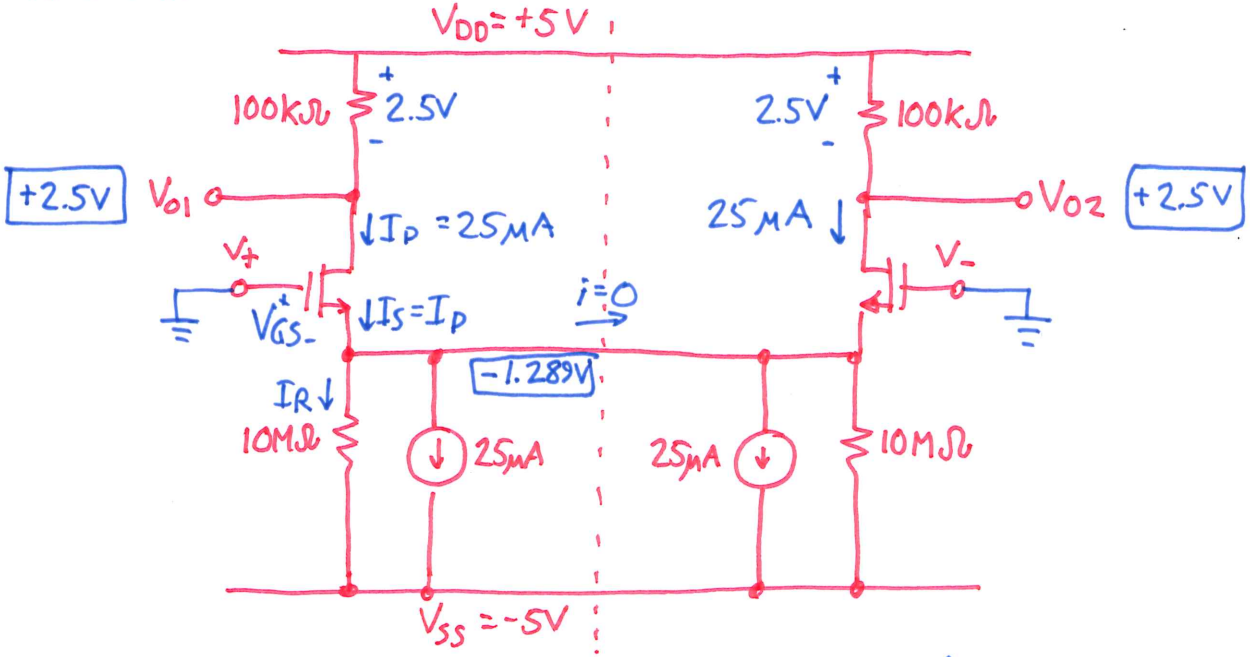
SQ LAW

$25\mu A = (3E-4)\underbrace{(V_{GS}-1V)}_{0.289\,V}{}^2 \Rightarrow V_{GS} = 1.289\,V$

FOR small signal

$g_m = \frac{2I_D}{V_{GS}-V_{TH}} = \frac{2\,25\mu A}{0.289} = 175\,\mu A/V$

REDRAW TO SHOW SYMMETRY:



DC OPERATING POINT $V_+ = V_- = 0$ (NO CM OR DM)

SYMMETRIC EXCITATION $i = 0$ ACROSS !

KCL AT SOURCE

$I_R + 25\mu A = I_D$

I_R: OHM'S LAW $\frac{-V_S + 5V}{10M\Omega}$ — ALSO NEED V_{GS} !

I_D: FROM SQUARE LAW (NEED V_{GS})

SYSTEM OF EQUATIONS WITH V_{GS}, V_{GS}^2

I_R SHOULD BE $< 25\mu A$

GUESS $V_{GS} \approx 1.5\,V \Rightarrow I_R = \frac{3.5V}{10M\Omega} = 0.35\mu A$ ($\approx 1\%$ OF $25\mu A$)

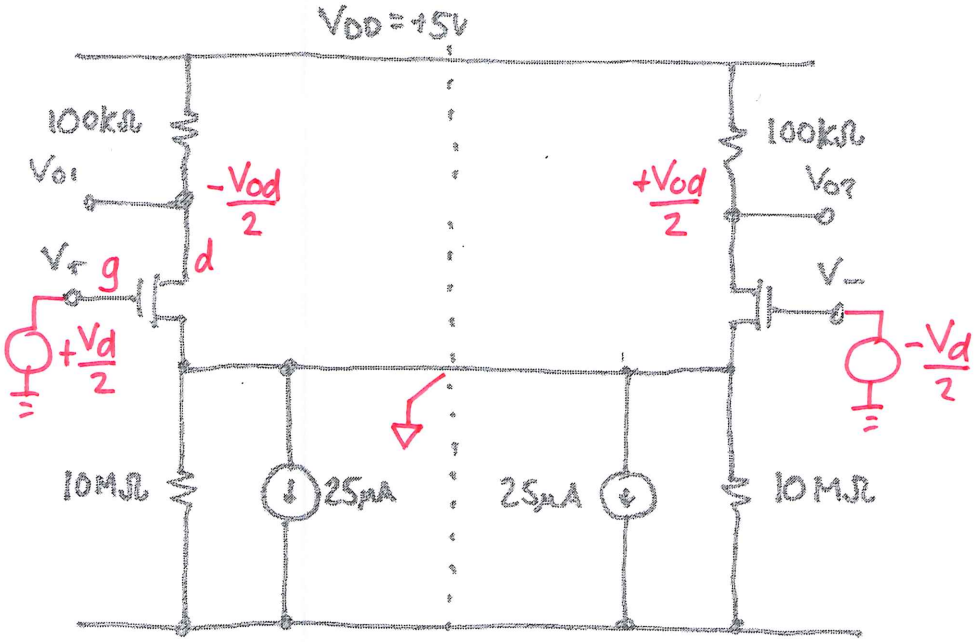
CHECK

REVISE

$I_R \ll 25\mu A \Rightarrow I_D \approx 25\mu A$

Differential mode

BREAK; CONNECT TO SIGNAL GND



$$-\frac{V_{od}}{2} = -g_m \underbrace{V_{gs}}_{\frac{V_d}{2}} 100\,k\Omega$$

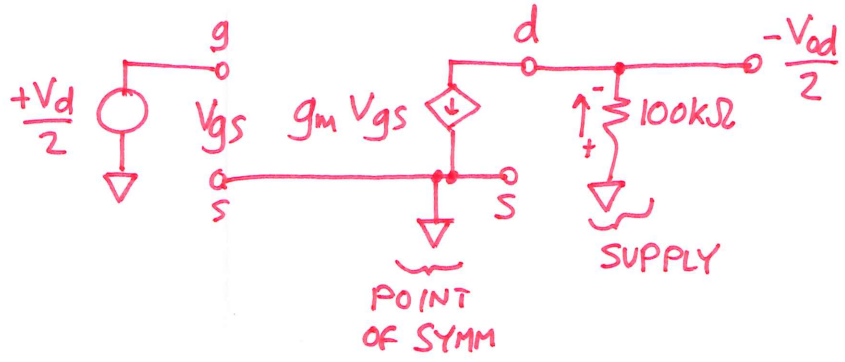
DIFFERENTIAL GAIN

$$\frac{V_{od}}{V_d} = g_m(100k\Omega)$$

$$= (175\mu A/V)(100k\Omega)$$

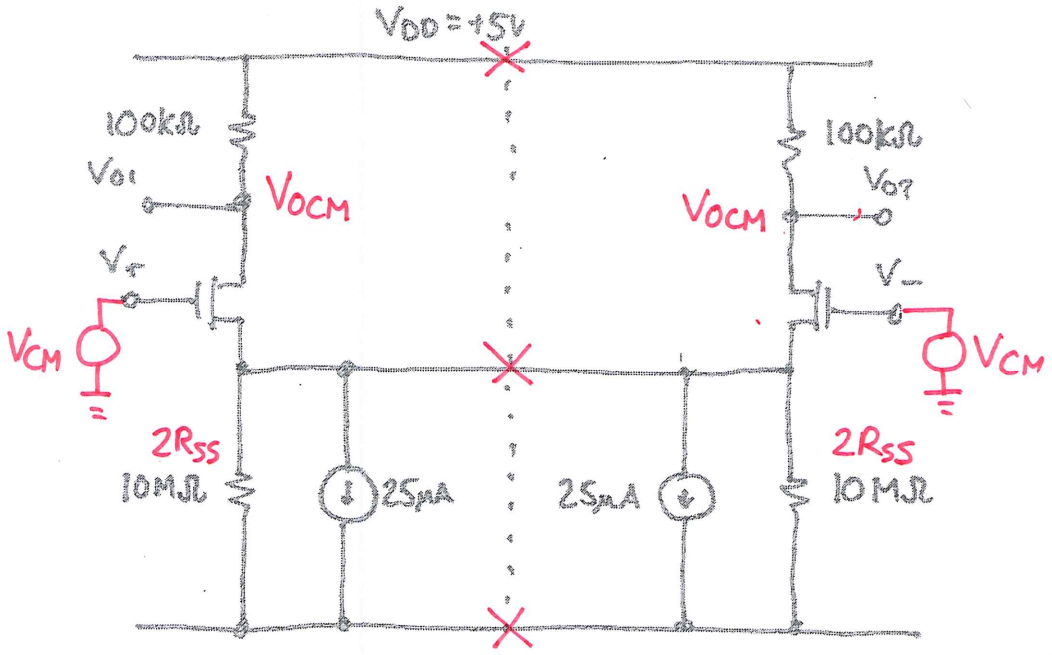
$$= 17.5$$

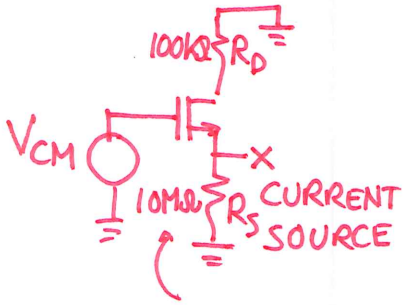
REDRAW WITH small signal MODEL



Common mode

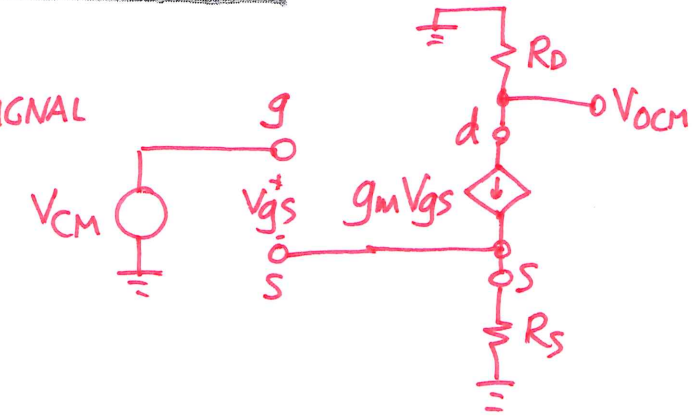
OPEN CONNECTED POINTS OF SYMMETRY





COMMON SOURCE AMPLIFIER WITH "SOURCE DEGENERATION"

SMALL SIGNAL ⇒



FULL ANALYSIS

$R_S >> R_D$

$$\frac{V_{OCM}}{V_{CM}} \approx \frac{-R_D}{R_S}$$

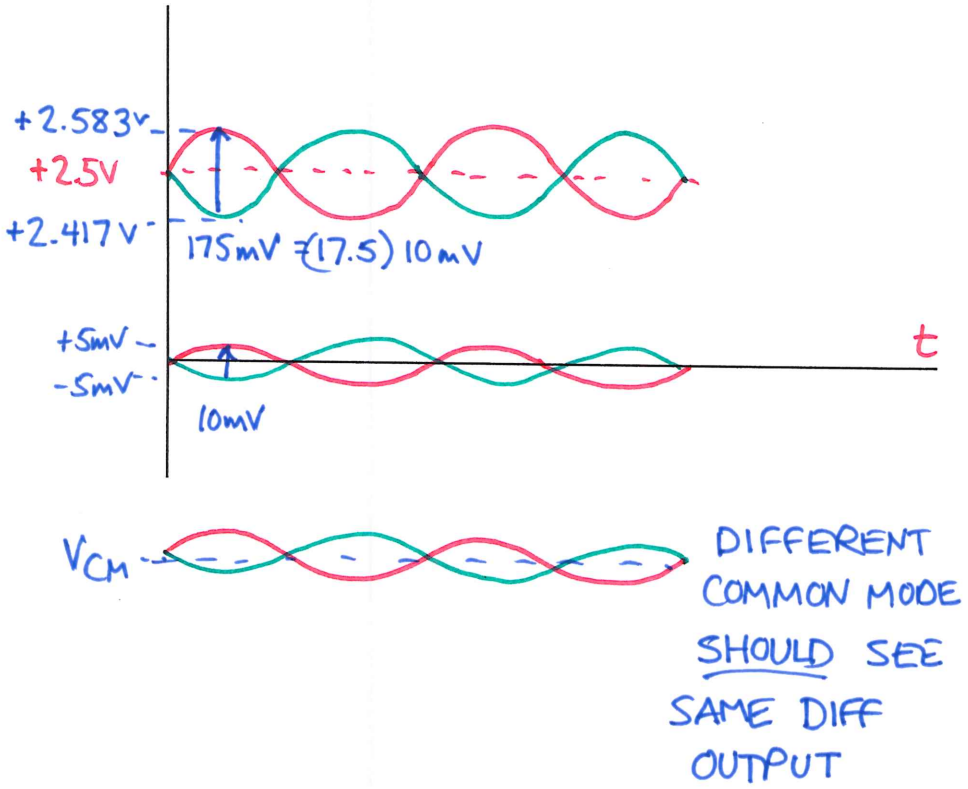
$$\frac{100k\Omega}{10M\Omega} \approx 0.01$$

CMR "COMMON MODE REJECTION"

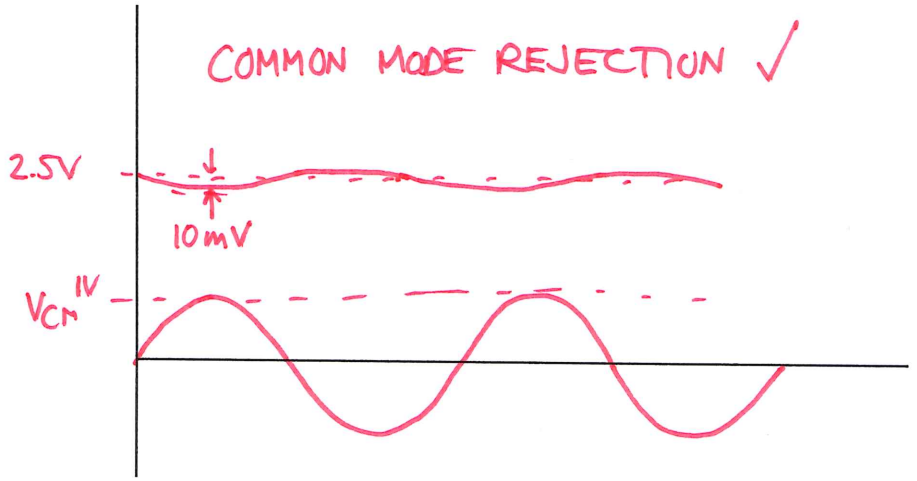
IDEAL: → 0

MAKE $R_S \to \infty$

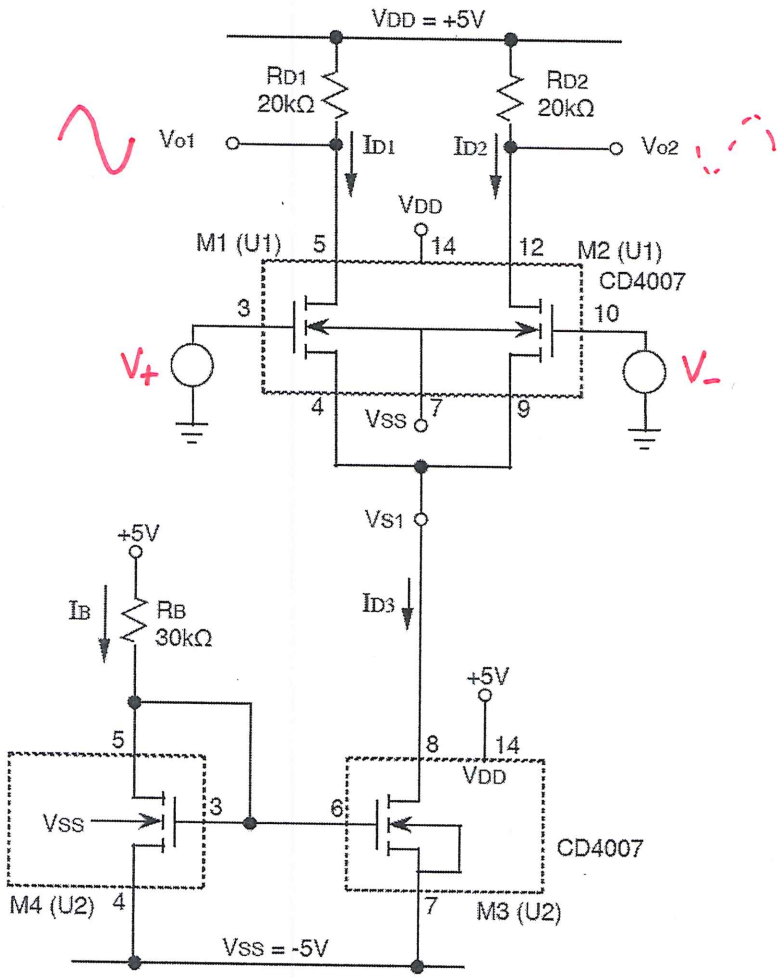
Outputs: Differential mode



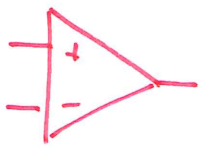
Outputs: Common mode



Op-amp requirements for differential amplifier



GOALS



$V_o = A(V_+ - V_-)$

✓ RESPOND TO DIFFERENCE

✗ HIGH GAIN

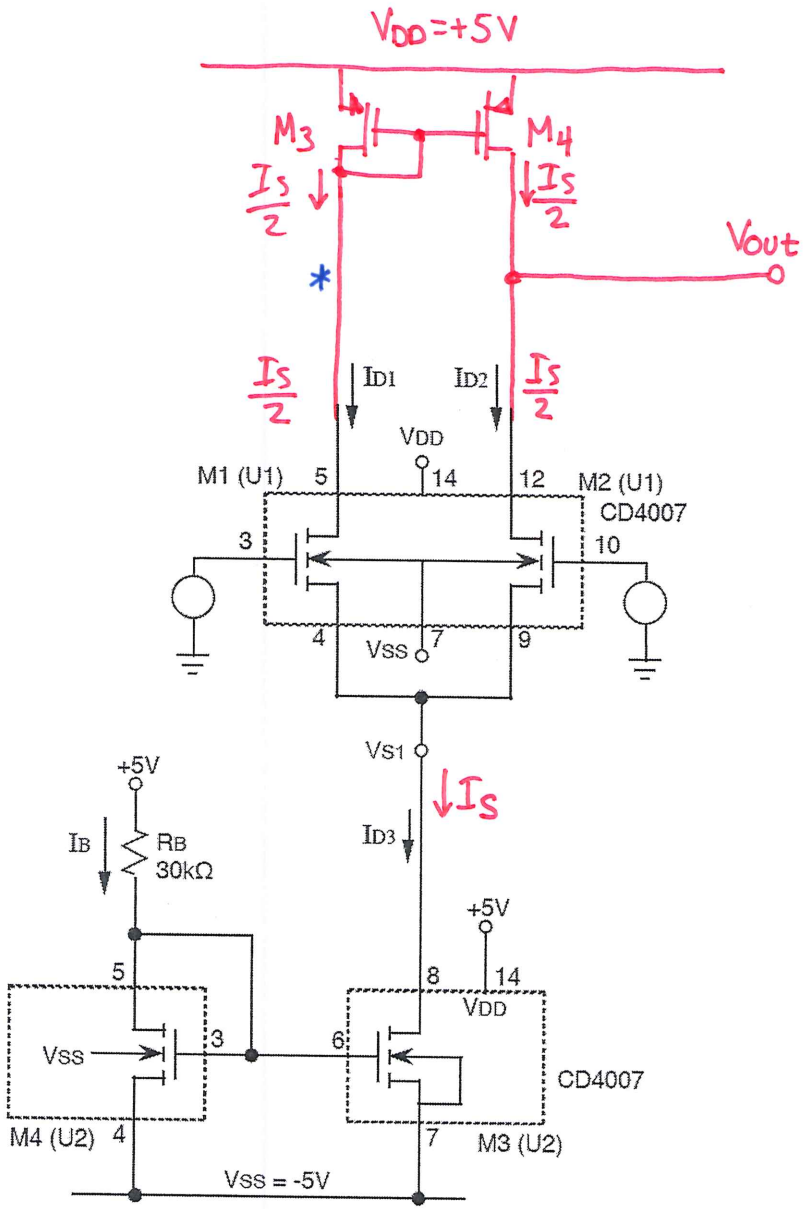
SINGLE-ENDED OUTPUT

GAIN $g_m R_D$ ~ 10-20

TAKE 1 SIDED OUTPUT

LOSE 2X OF GAIN

ACTIVE LOAD ?



ACTIVE LOAD IN DRAIN OF M_2

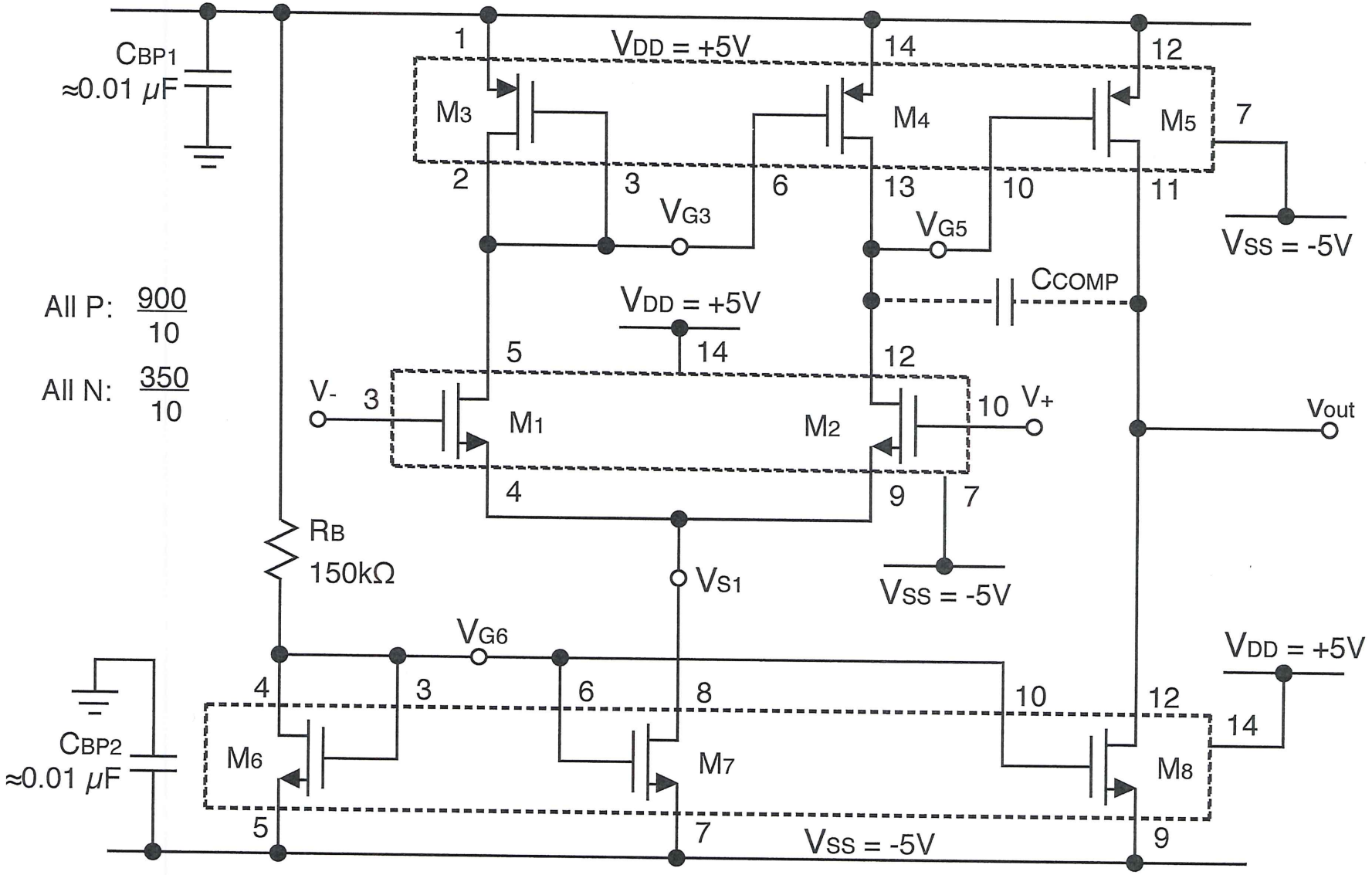
HIGH GAIN ADD M_4 AS ACTIVE LOAD
MUST BE PMOS (HIGH r_o LOOKING INTO DRAIN)

M_3: DIODE CONNECTED FOR MIRROR

HOW TO DO DC BIAS?

DC BIAS!? * USE "OTHER" $I_S/2$ FROM M_4
AS INPUT TO MIRROR

Lab 8 op-amp:


CBP1
≈0.01 μF
1
VDD = +5V
14
12
M3
M4
M5
7
2
3
6
13
10
11
VG3
VG5
VSS = -5V
All P: 900/10
All N: 350/10
CCOMP
VDD = +5V
5
14
12
V-
3
M1
M2
10
V+
Vout
4
9
7
RB
150kΩ
VS1
VSS = -5V
VG6
VDD = +5V
4
3
6
8
10
12
14
CBP2
≈0.01 μF
M6
M7
M8
5
7
VSS = -5V
9