ECE4902 Lecture 11

2-Stage Op-Amp
- Finish Design Example
- Simulation results

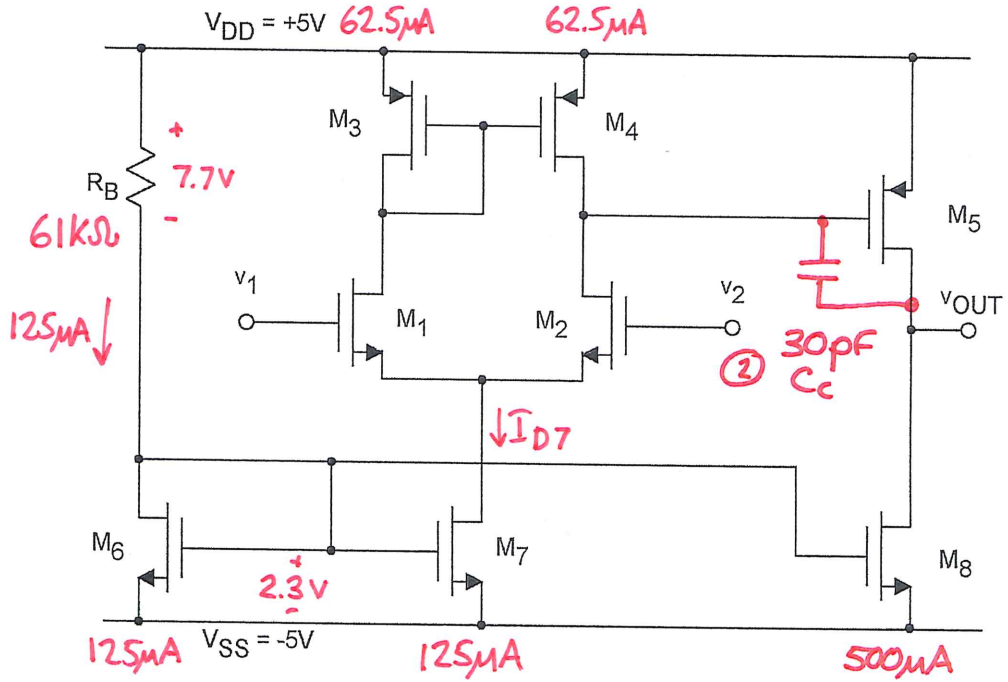
Improving Performance
- Cascode

Handout:
Design Example

Specifying Op-Amp Design:

MOSFET	DC Bias		Size ①		Remarks
	ID [µA]	$V_{GS} - V_{TH}$	W [µm]	L [µm]	
M1	62.5µA	0.25V	380	10	
M2	62.5µA	0.25V	380	10	
M3	62.5µA	-0.4V	900	10	
M4	62.5µA	-0.4V	900	10	
M5	500µA	-0.4V	7200	10	
M6	125µA	0.4V	600	10	CHOOSE SAME W AS M_7: SAME I_D
M7	125µA	0.4V	600	10	I_{D7} FROM SLEW RATE, W SCALED FROM M_8
M8	500µA	0.4V	2400	10	

③ FOR $R_B = \frac{7.7V}{125\mu A} = 61k\Omega$



Parameter	N-channel	P-channel	Units
V_{TH}	+1.90	-1.60	V
μC_{ox}	2.6E-5	9.1E-6	A/V^2
λ (L=10µm)	0.05	0.028	V^{-1}

① MINIMIZE AREA (CD4007 PARAMETERS) ALL $L = 10\mu m$
(COULD CHANGE LATER; HAVE TO START SOMEWHERE!)

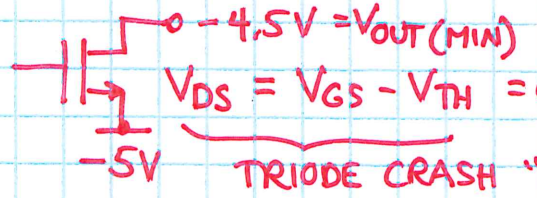
② CHOOSE $C_c = 30\,pF$ [SEE ECE529C; NOISE CONSIDERATIONS]

③ M_8 MUST ALWAYS CONDUCT MAX CURRENT

$450\mu A \Rightarrow 500\mu A = I_{D8}$

④ OUTPUT SWINGS DETERMINED BY TRIODE CRASH

M_8:



SAME FOR M_5

PMOS: $-0.4V$

⑤ W_8 FROM SQUARE LAW

$$500\mu A = \frac{2.6E\text{-}5}{2}\frac{W}{10}(0.4V)^2 \Rightarrow 2400\mu m$$

W_5

$$500\mu A = \frac{9.1E\text{-}6}{2}\frac{W}{10}(-0.4V)^2 \Rightarrow 7200\mu m$$

⑥ SLEW RATE: I_{D7} (DIFF PAIR BIAS), $C_c = 30pF$

$$SR = \frac{I_{BIAS}}{C_c}$$

$$\left(2.83E{+}6\,\frac{V}{sec}\right)(30\,pF) = 90\mu A \xrightarrow{\text{MARGIN}} 125\mu A$$

M_7, M_8 HAVE SAME V_{GS}, L: SCALE I_D BY WIDTH $\frac{I_{D8}}{I_{D7}} = \frac{W_8}{W_7}$

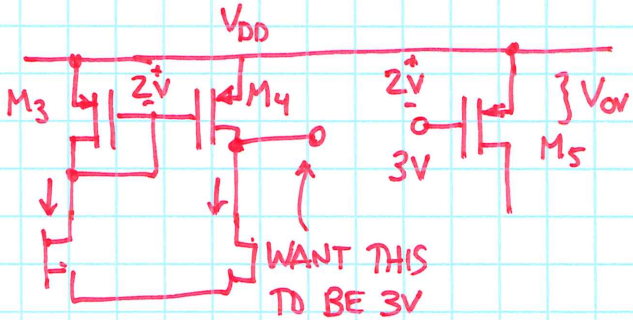
$$\frac{500\mu A}{125\mu A} = \frac{2400}{W_7} \Rightarrow W_7 = \frac{1}{4}(2400)$$

⑦ I_{D7} MUST SPLIT BY SYMMETRY IN DIFF PAIR (M_1, M_2) AND MIRROR (M_3, M_4)

⑧ M_6, M_7 SAME

⑩ M_3, M_4 FROM DC BIAS MATCHING

BALANCE: M_3, M_4 HAVE SAME V_{DS}



SIZE M_3, M_4 FOR SAME V_{GS} AS M_5; SCALE WIDTHS

$$W_4 = \frac{1}{8} W_5$$

$$\frac{I_{D4}}{I_{D5}} = \frac{W_4}{W_5} \Rightarrow \frac{62.5\mu A}{500\mu A} = \frac{1}{8}$$

⑪ INPUT STAGE: UNITY GAIN FREQUENCY

$$f_T = \frac{g_{m1}}{2\pi C_C} \Rightarrow 388\,kHz = \frac{g_{m1}}{2\pi (30pF)} \Rightarrow g_{m1} \geq 73 \frac{\mu A}{V}$$

HIGHER: FASTER f_T

DEVICE:

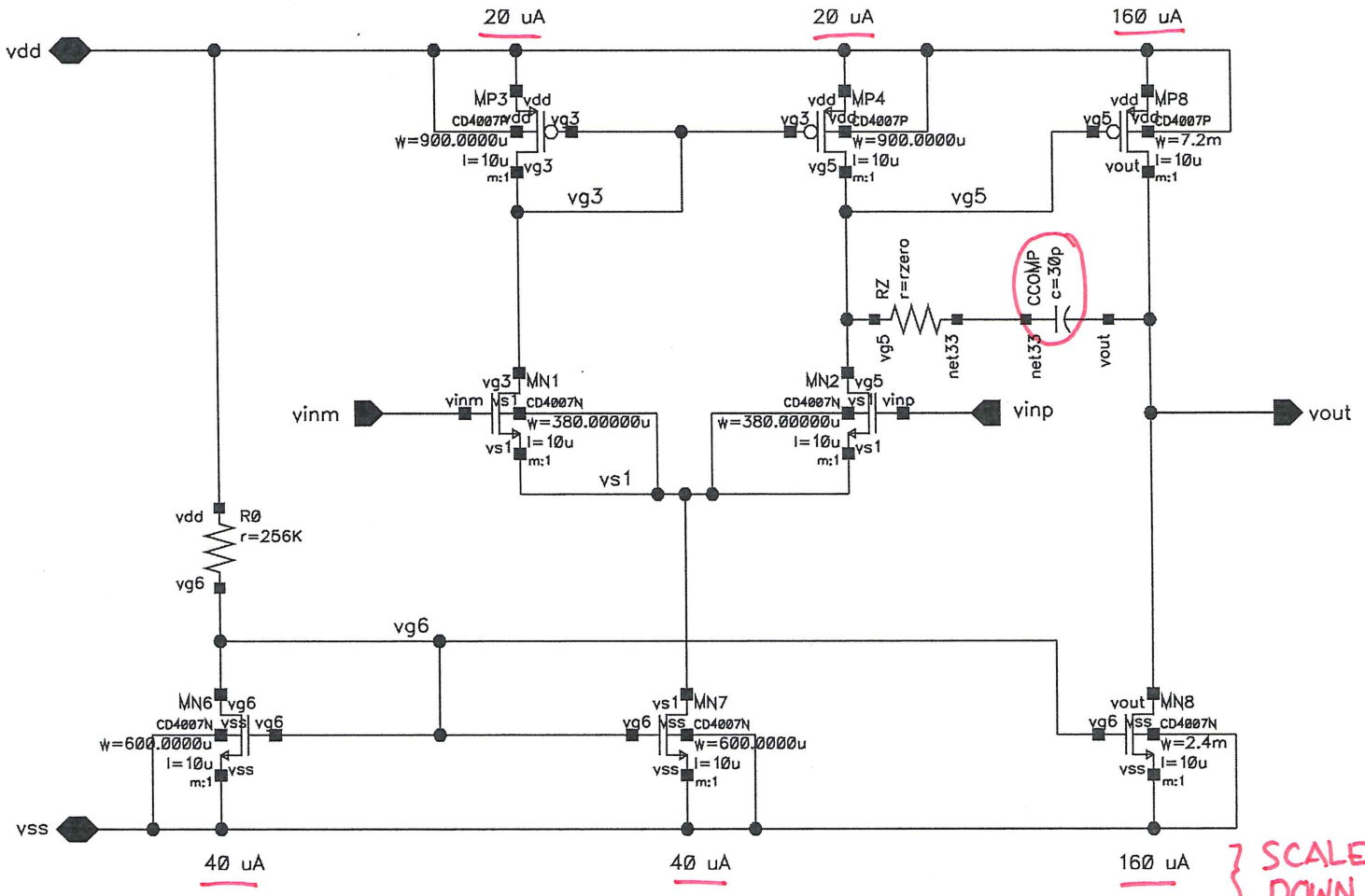
$$g_m = \frac{2 I_D}{V_{OV1}} \Rightarrow 73 \frac{\mu A}{V} = \frac{2(62.5\mu A)}{V_{OV}} \Rightarrow V_{OV} \leq 1.71V$$

CHOOSE V_{OV} SMALLER

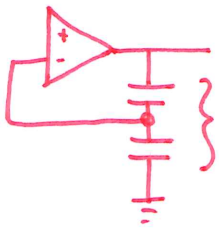
- BETTER g_m/I_D EFFICIENCY
- BETTER INPUT CM RANGE

$V_{OV} = 0.25$ (BEST g_m/I_D)

$$62.5\,\mu A = \frac{2.6E\text{-}5}{2} \frac{W_1}{10} (0.25V)^2 \Rightarrow W_1 = 380$$



CHANGES FOR ON-CHIP OP-AMP



} CAPACITIVE FEEDBACK: NO DC CURRENT

} SCALED DOWN BY 3X (SAVE POWER)

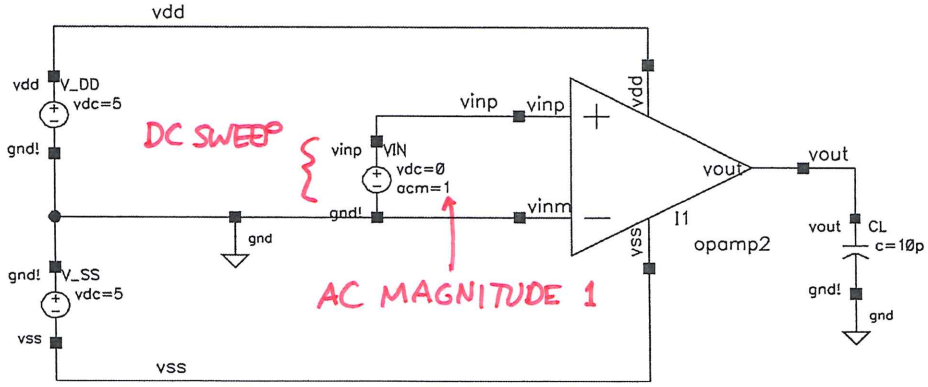
g_m FOR INPUT STAGE

$$g_m = \sqrt{2(20\mu A)(2.6E\text{-}5)\frac{380}{10}}$$

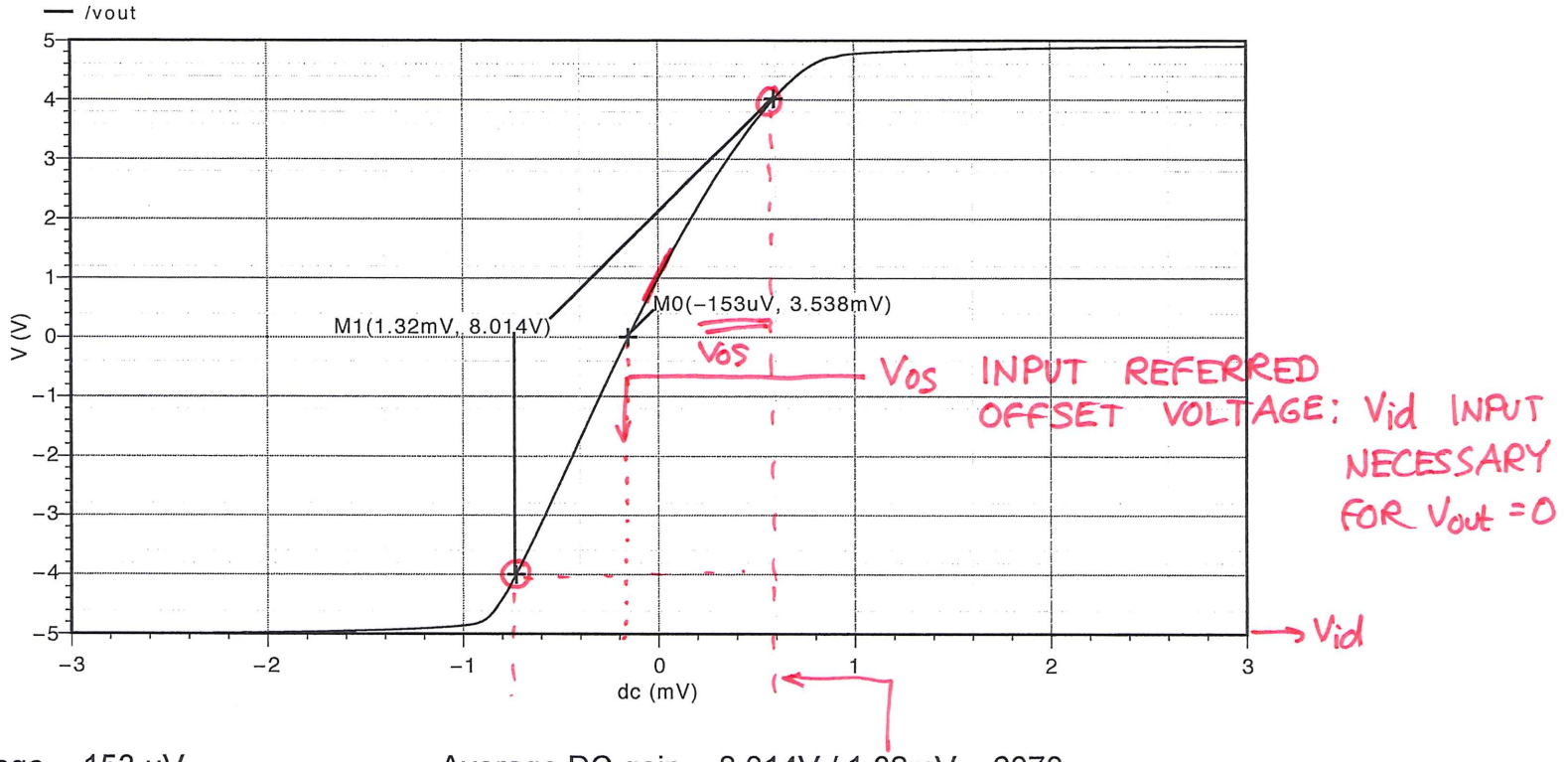
$$= 200\mu A/V$$

PREDICTED f_T: $\frac{g_m}{2\pi C_c} = \frac{200\mu A/V}{2\pi(30pF)} = 1.06\ MHz > 388\ kHz$ ✓

Open Loop Test Simulation



Open Loop DC response



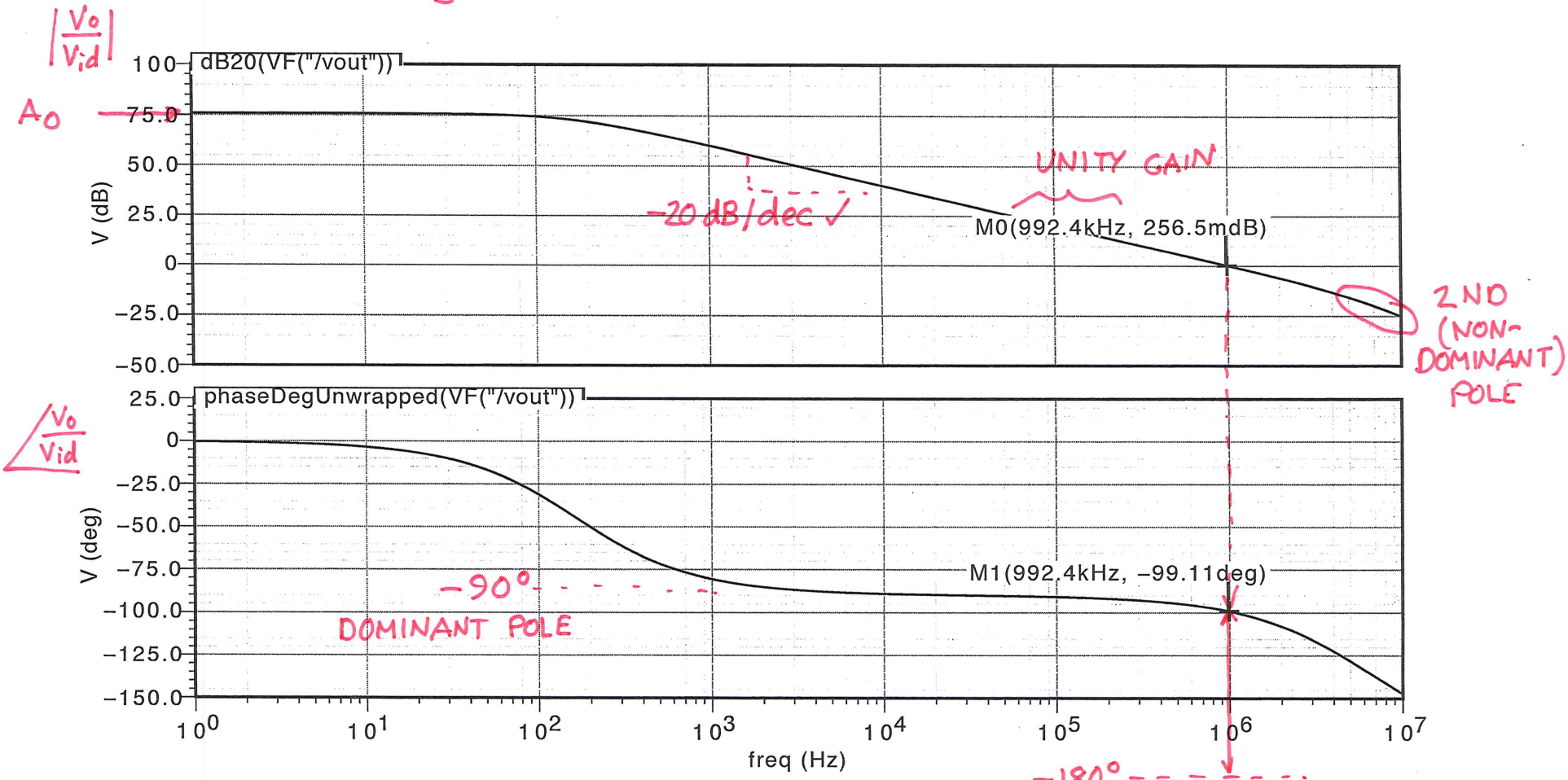
Systematic Offset Voltage -153 µV

Average DC gain = 8.014V / 1.32mV = 6070

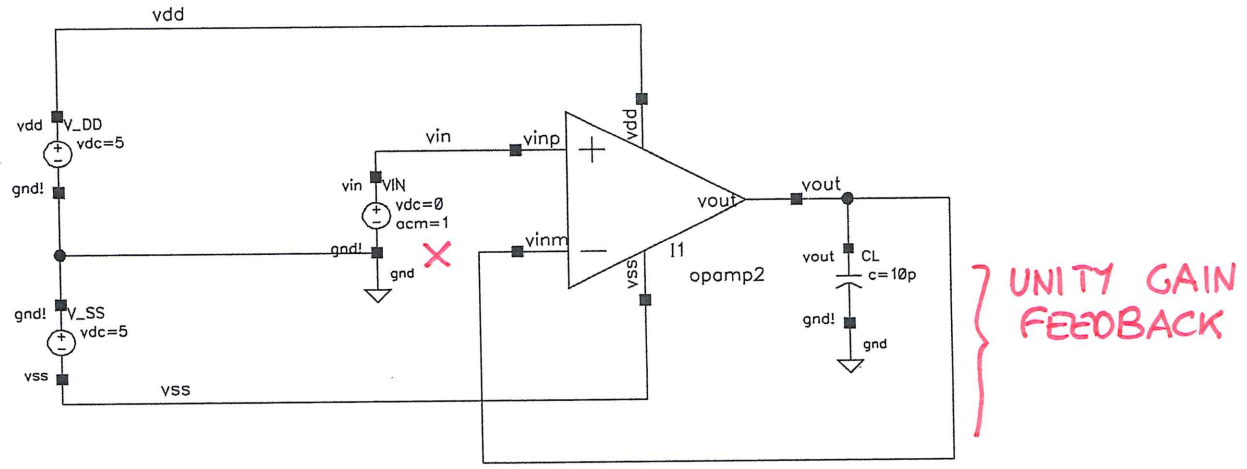
Open Loop AC response

>2000 ✓

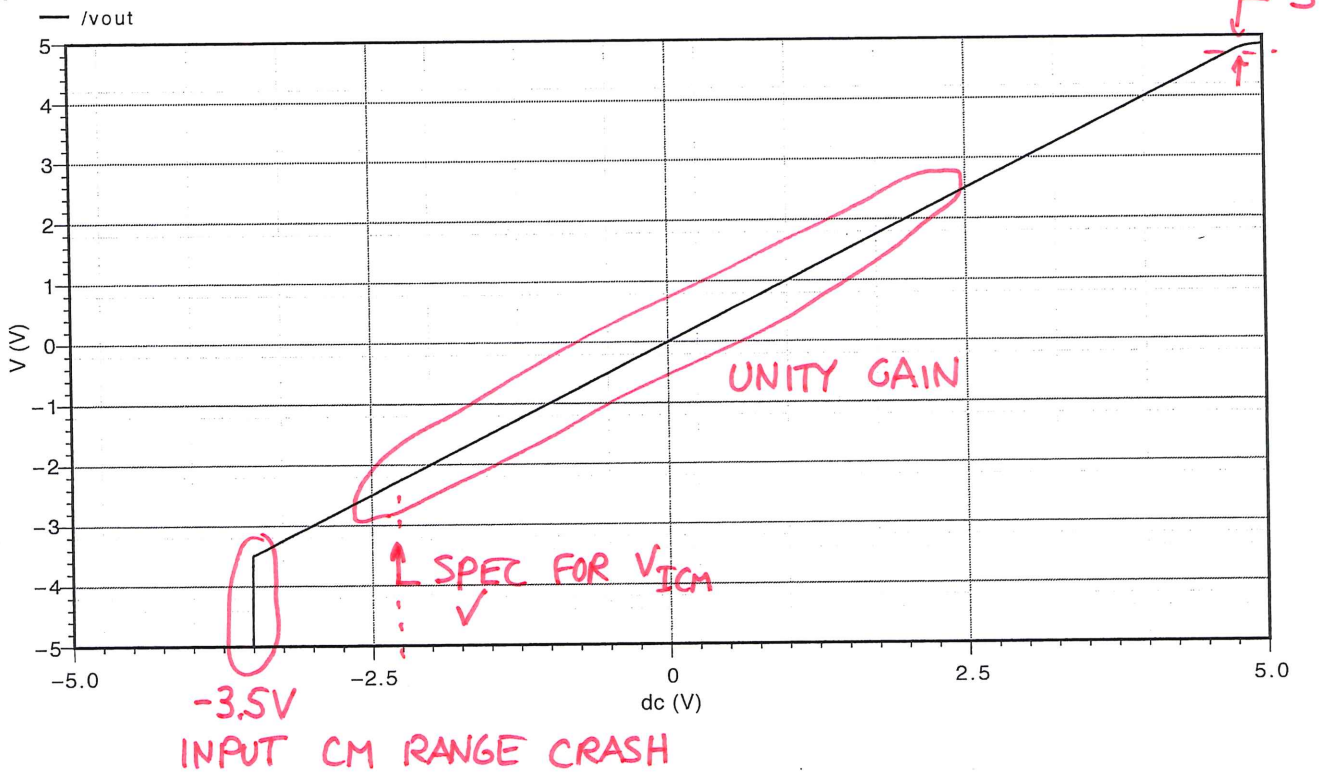
$20 \log(6070) = \cancel{78.16}$ 75.6 dB ✓



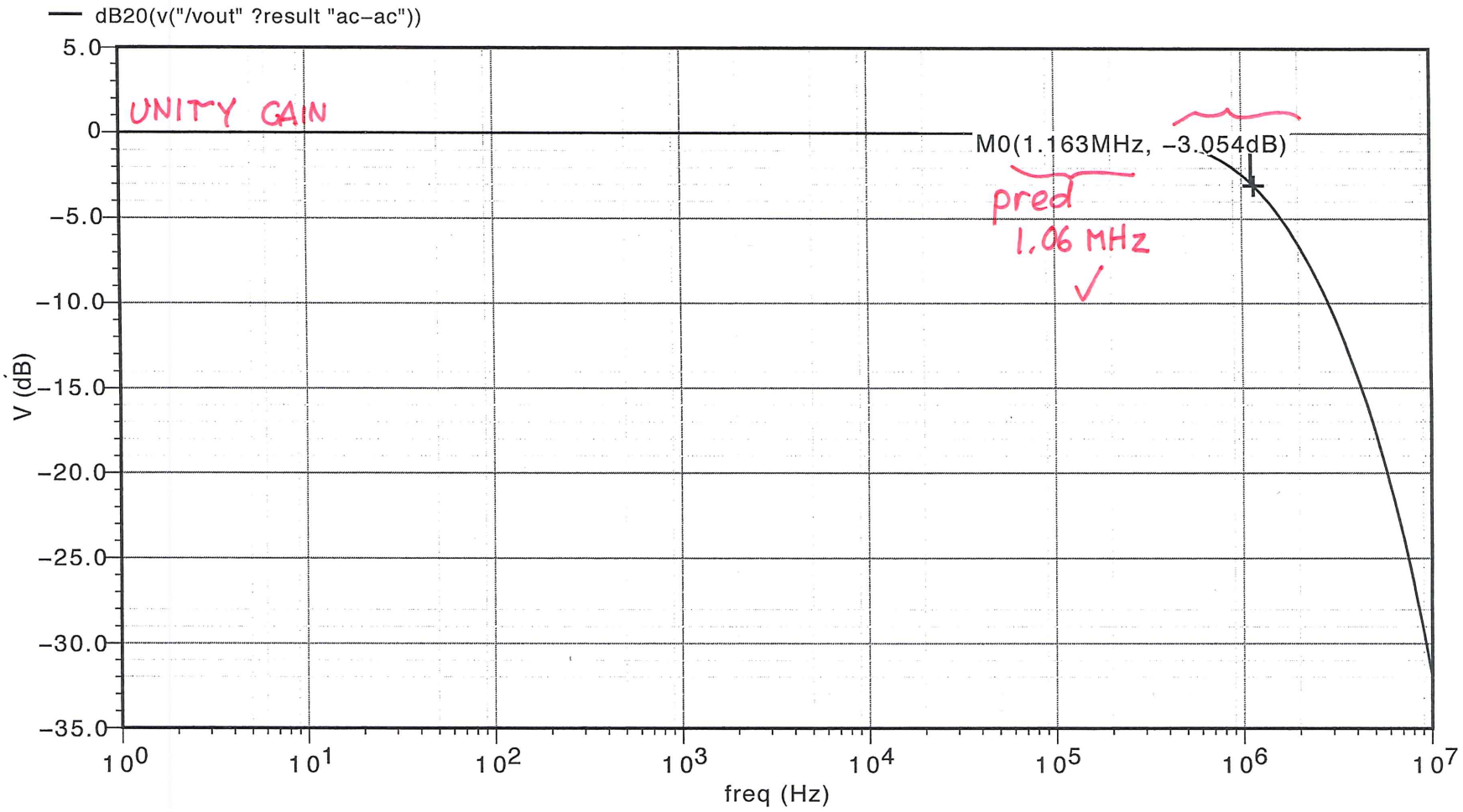
Closed Loop Simulations



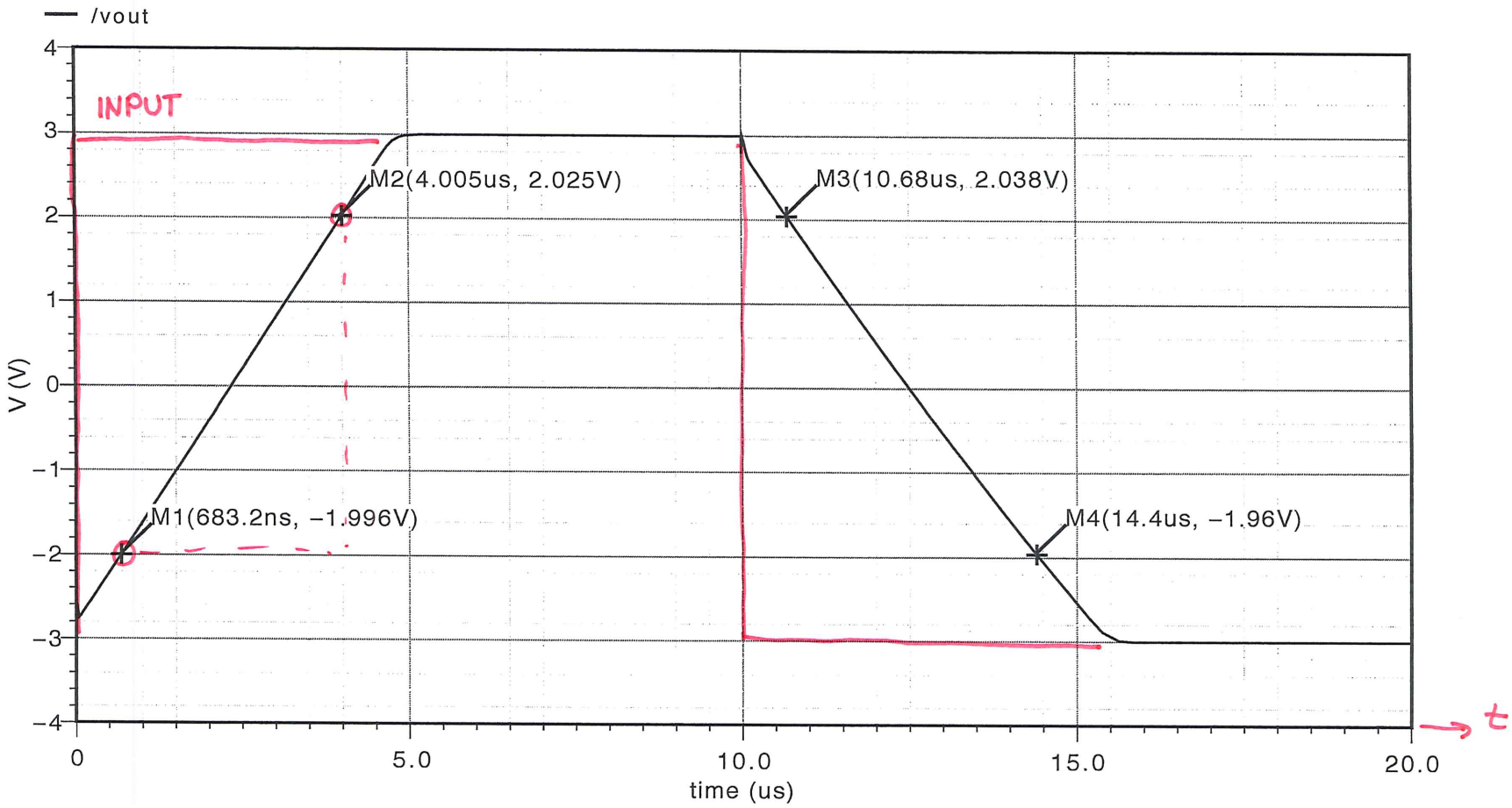
Closed Loop DC Sweep



Closed Loop Transfer Function (Unity Gain)



Closed Loop Step Response (Large Signal) TRANSIENT ANALYSIS



Rising slew rate 4V / 3.31µs = 1.21 V / µs

Falling slew rate 4V / 3.72µs = 1.08 V / µs

PREDICTED: $\frac{I_{D7}}{C_c} = \frac{40\mu A}{30pF} = 1.33 \frac{V}{\mu sec}$ ✓

2 REASONS: PARASITIC CAP ADDS TO C_c
↗ ↘ DIFFERENT (SEE SOLOMON OP-AMP PAPER)

How to Increase Open Loop Gain?