

ECE4902 Lecture 11

2-Stage Op-Amp

Finish Design Example

Simulation results

Improving Performance

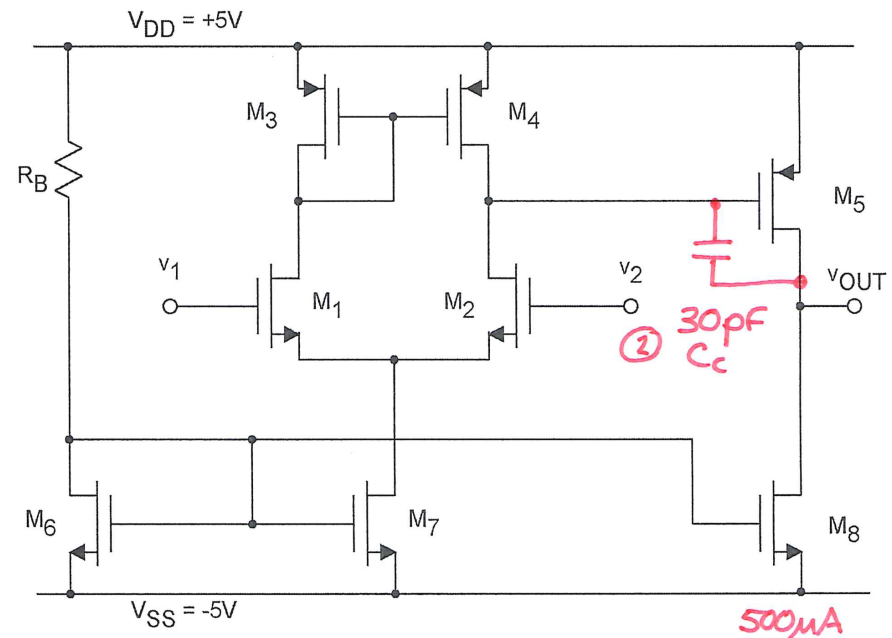
Cascode

Handout:

Design Example

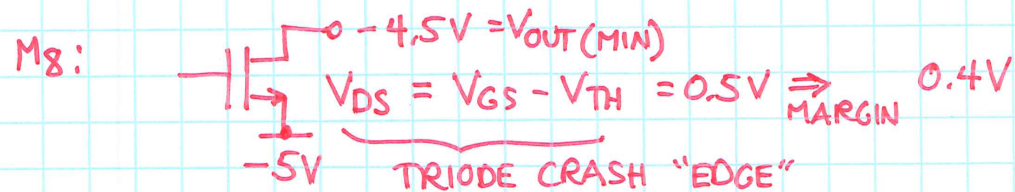
Specifying Op-Amp Design:

MOSFET	DC Bias		Size ①		Remarks
	ID [μ A]	$V_{GS} - V_{TH}$	W [μ m]	L [μ m]	
M1				10	
M2				10	
M3				10	
M4				10	
M5	500 μ A	④ -0.4V	⑤ 7200	10	
M6		0.4V		10	
M7		0.4V		10	
M8	③ 500 μ A	④ 0.4V	⑤ 2400	10	



Parameter	N-channel	P-channel	Units
V_{TH}	+1.90	-1.60	V
μC_{ox}	2.6E-5	9.1E-6	A/V ²
λ (L=10 μ m)	0.05	0.028	V ⁻¹

- ① MINIMIZE AREA (CD4007 PARAMETERS) ALL $L = 10\mu\text{m}$
(COULD CHANGE LATER; HAVE TO START SOMEWHERE!)
- ② CHOOSE $C_c = 30\text{ pF}$ [SEE ECE529C; NOISE CONSIDERATIONS]
- ③ M_8 MUST ALWAYS CONDUCT MAX CURRENT
 $450\mu\text{A} \Rightarrow 500\mu\text{A} = I_{D8}$
- ④ OUTPUT SWINGS DETERMINED BY TRIODE CRASH



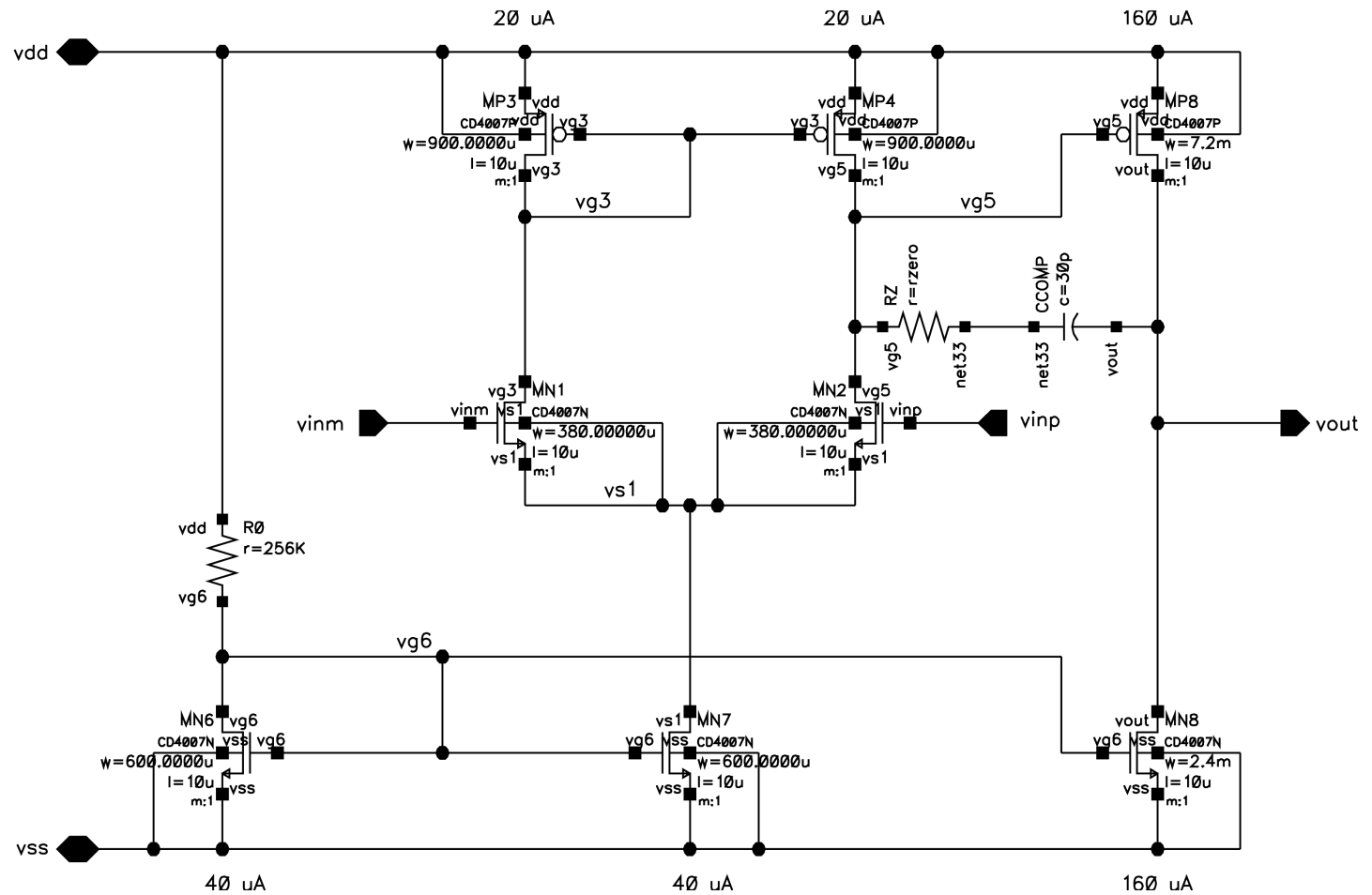
SAME FOR M_5
PMOS: -0.4V

- ⑤ W_8 FROM SQUARE LAW

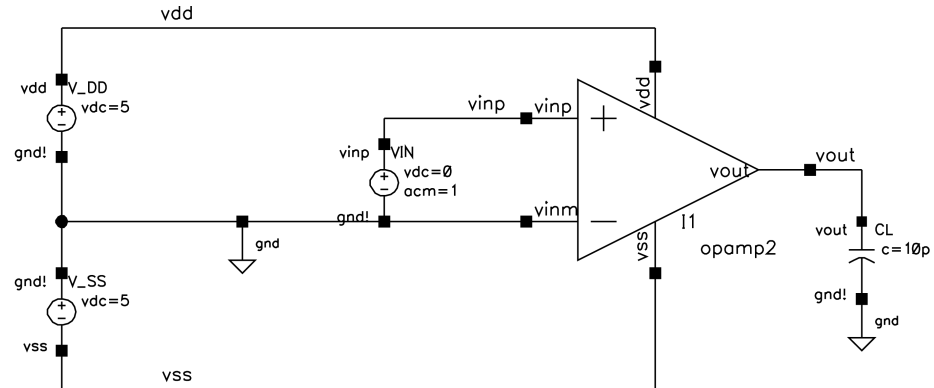
$$500\mu\text{A} = \frac{2.6\text{E-5}}{2} \frac{W}{10} (0.4\text{V})^2 = 2400\mu\text{m}$$

$$500\mu\text{A} = \frac{9.1\text{E-6}}{2} \frac{W}{10} (-0.4\text{V})^2 \Rightarrow 7200\mu\text{m}$$

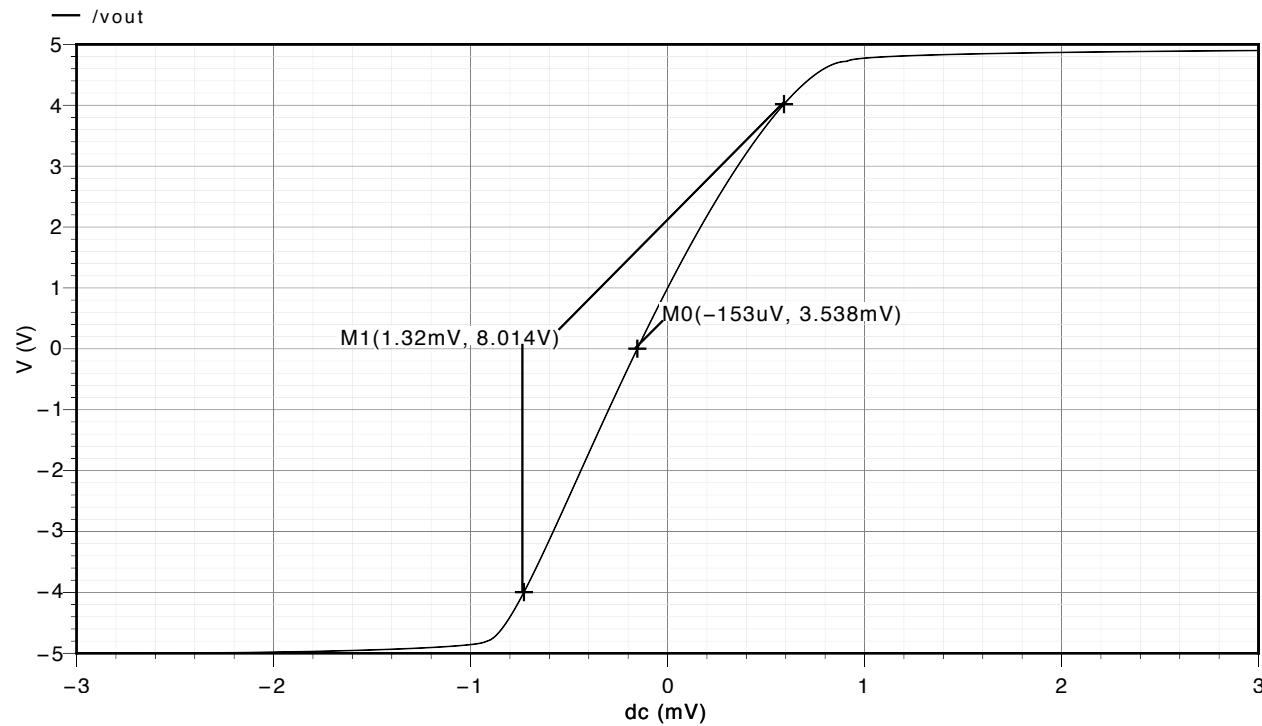
Op-Amp Design



Open Loop Test Simulation



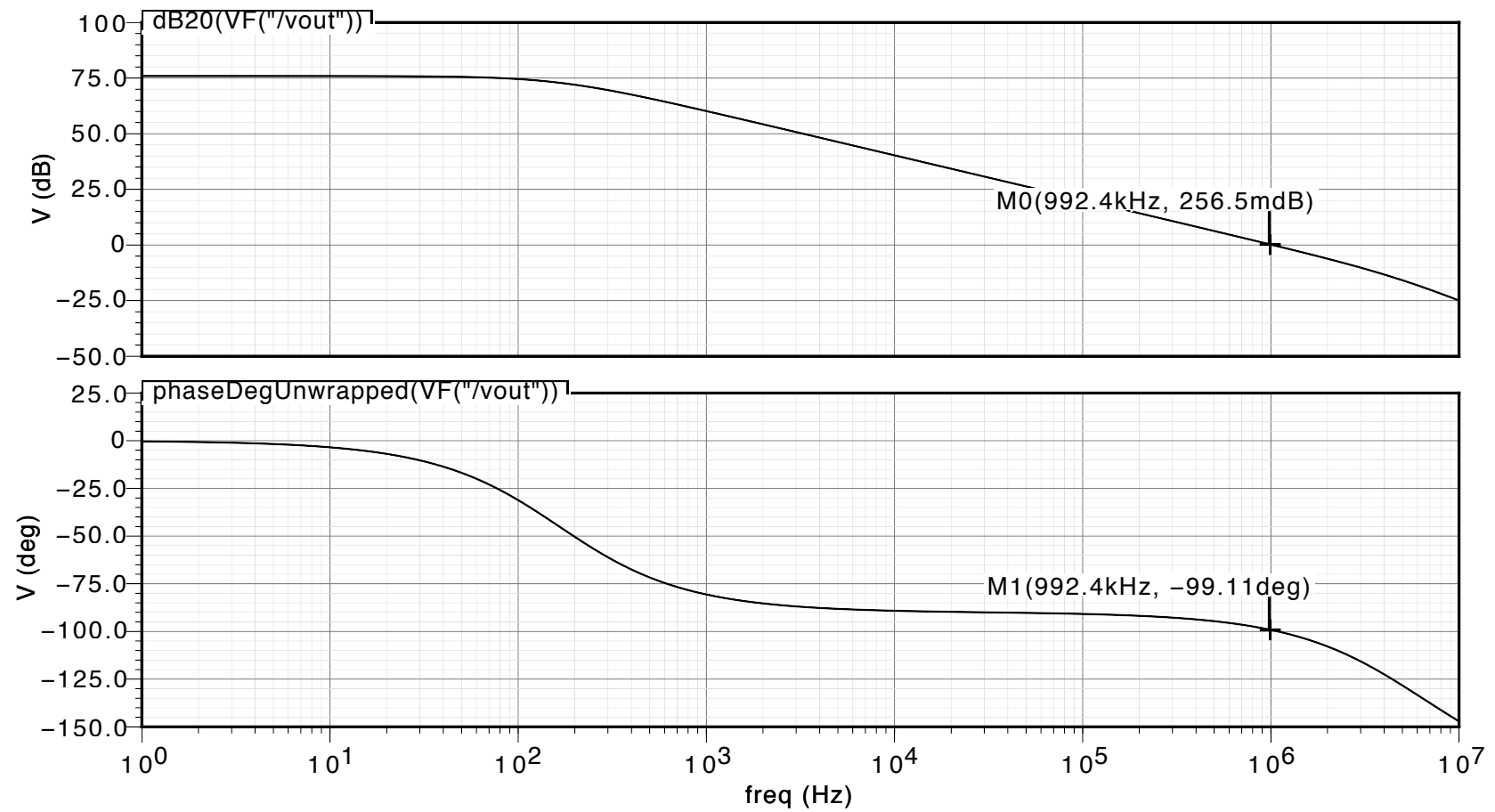
Open Loop DC response



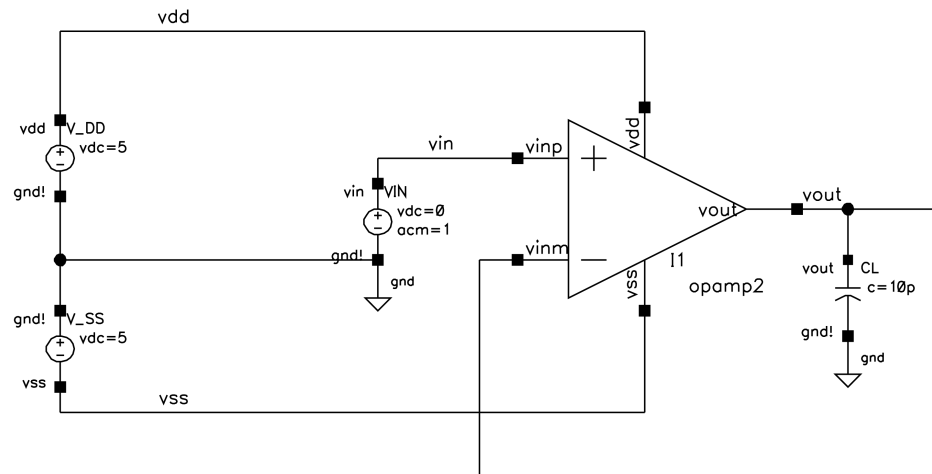
Systematic Offset Voltage -153 μ V

Average DC gain = $8.014\text{V} / 1.32\text{mV} = 6070$

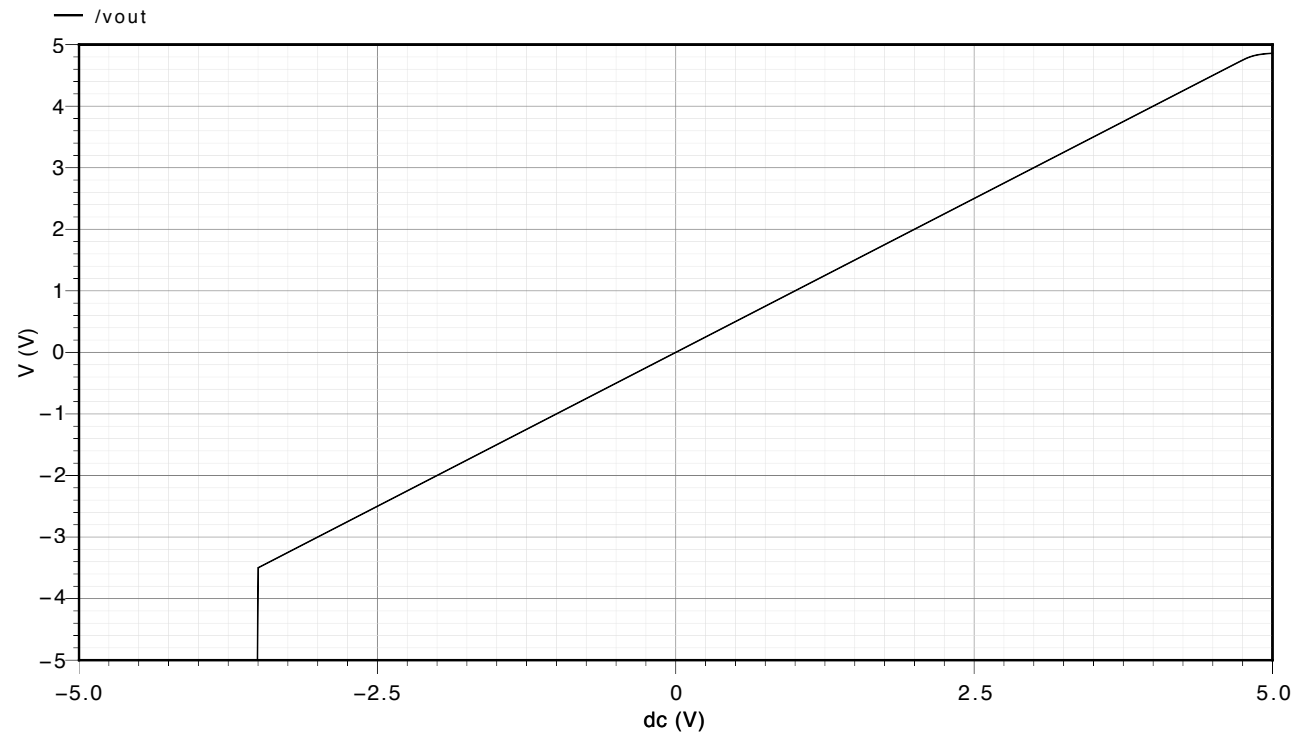
Open Loop AC response



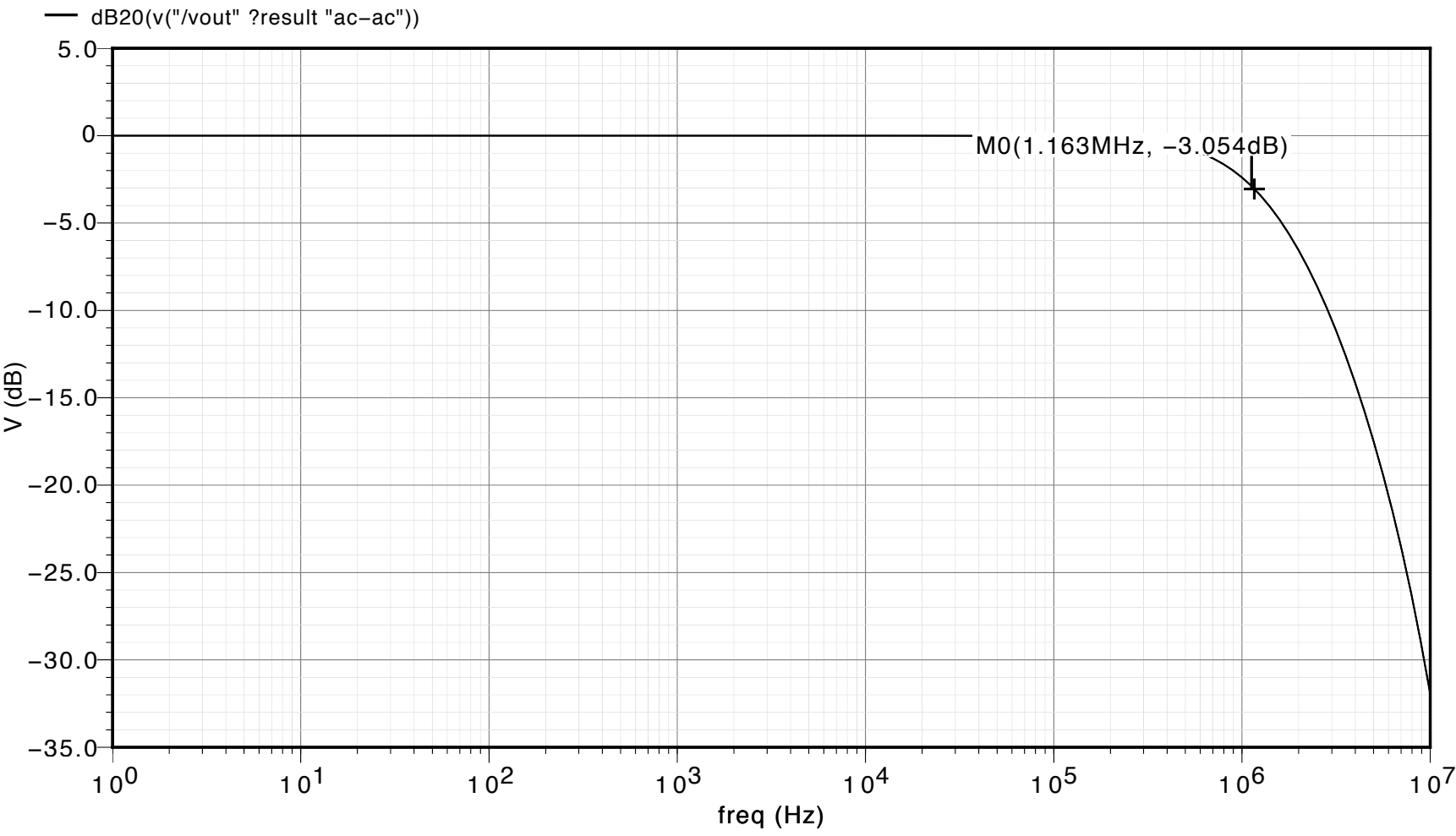
Closed Loop Simulations



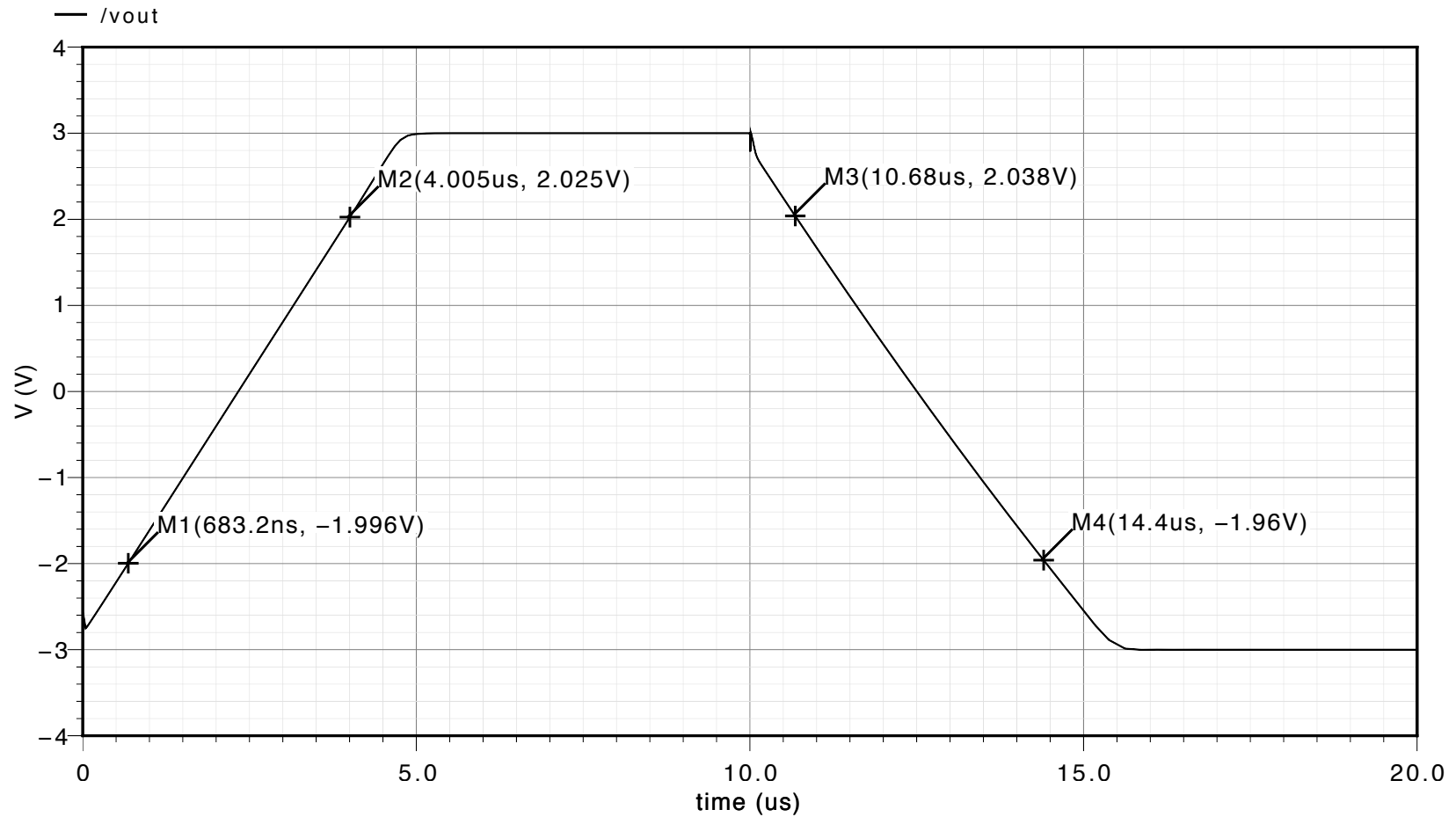
Closed Loop DC Sweep



Closed Loop Transfer Function (Unity Gain)



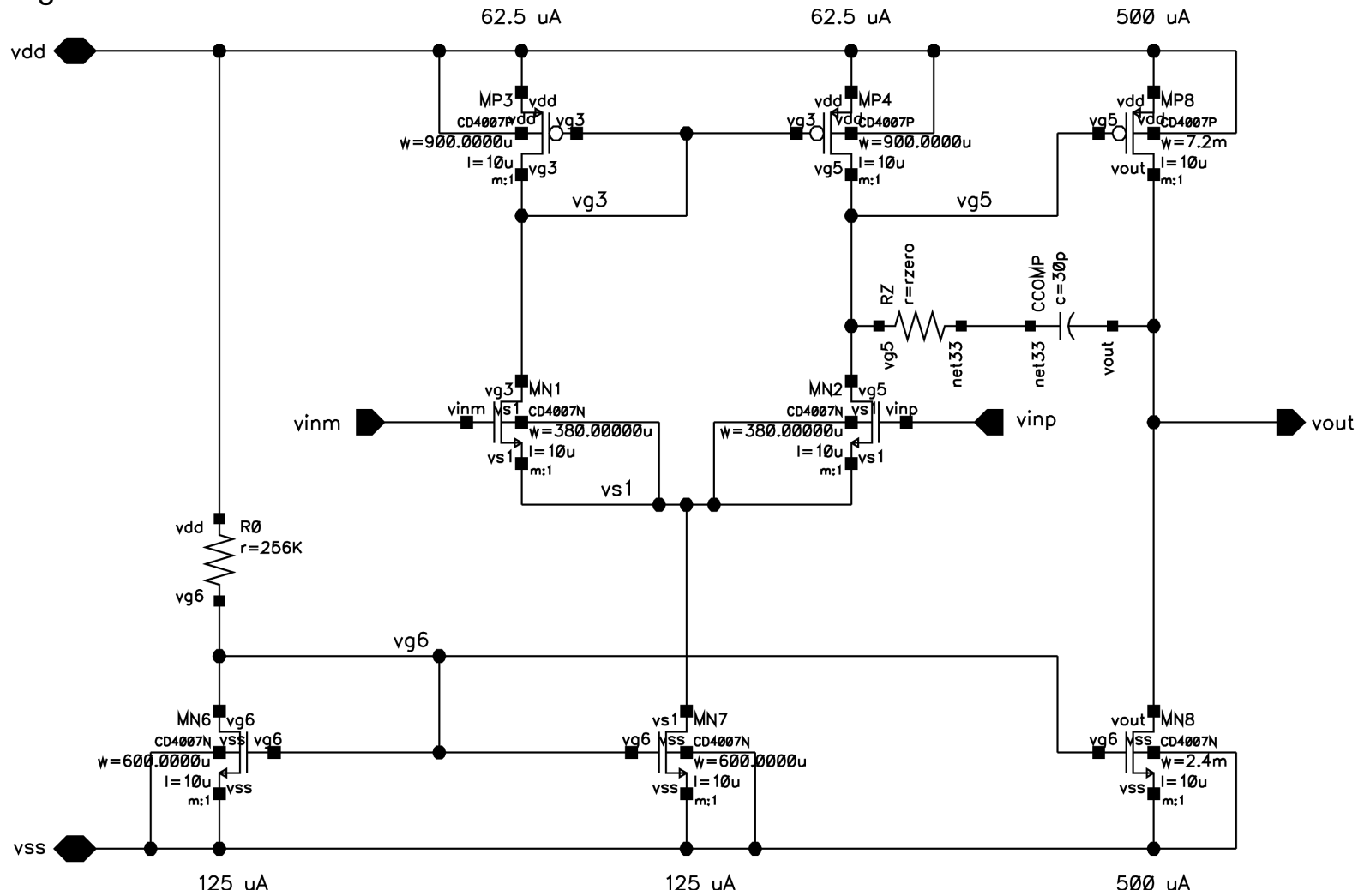
Closed Loop Step Response (Large Signal)



Rising slew rate $4V / 3.31\mu s = 1.21 V / \mu s$

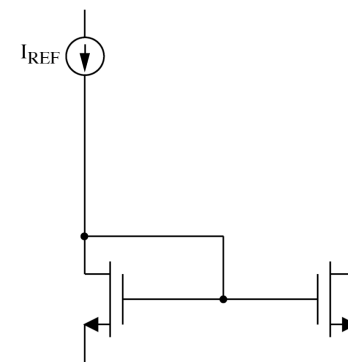
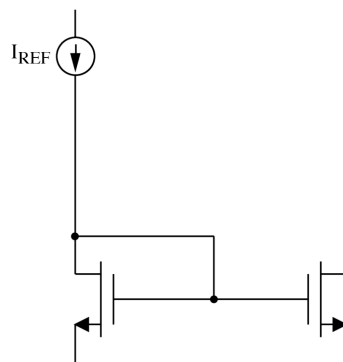
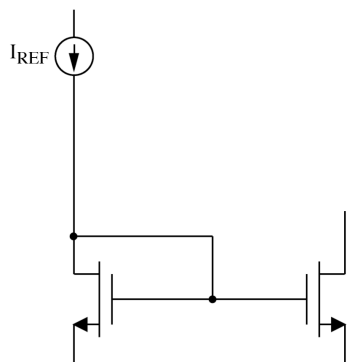
Falling slew rate $4V / 3.72\mu s = 1.08 V / \mu s$

Op-Amp Design

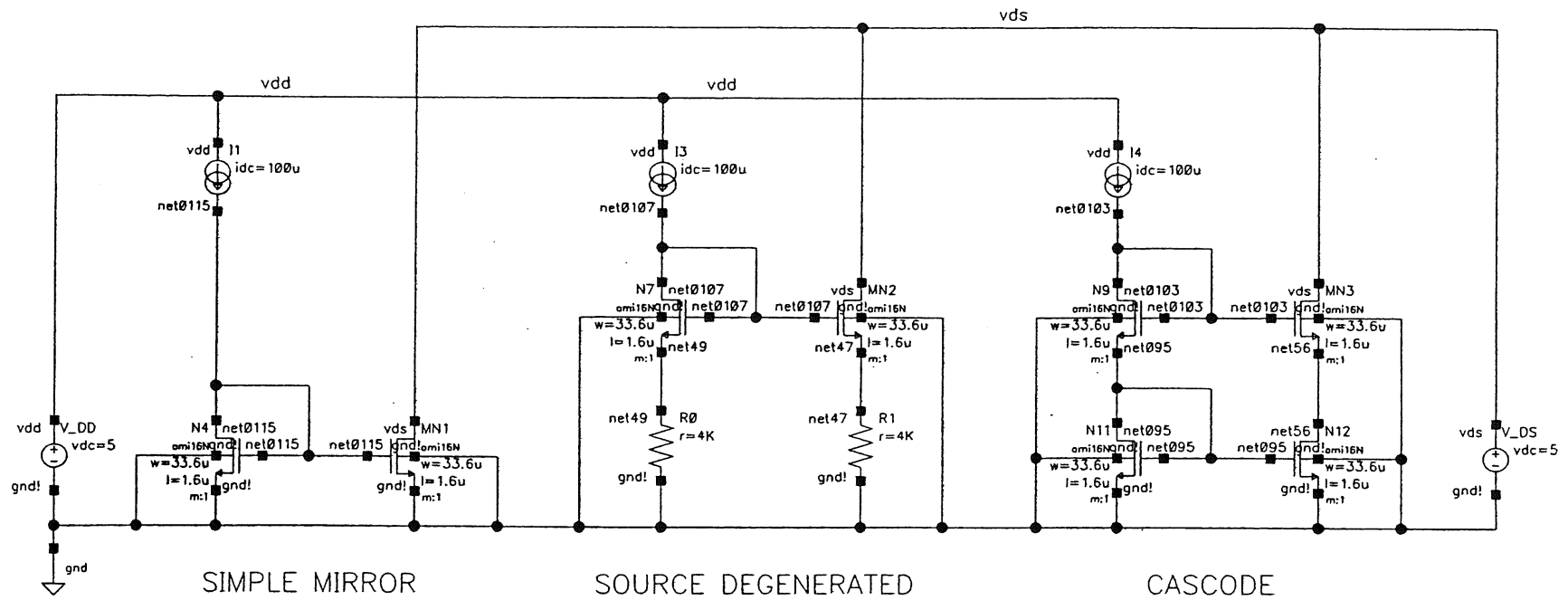


How to Increase Open Loop Gain?

Cascode Current Source Development



Current source comparison: Simulation



ID vs. V_DS SWEEP COMPARISON: SIMPLE MIRROR – SOURCE DEGENERATED – CASCODE

DC Response

