ECE4902 Lecture 12

How to Increase Open Loop Gain?

Improving Performance: Cascode Op-amp *

Tradeoff: + Higher node impedance

\- Reduced signal swing

2-Stage Op-Amp

CL, Phase Margin Issue

1-stage op-amp (Johns & Martin 6.2)

Improving Performance: Cascode

* Bandgap Voltage Reference

(* Optional Lab Circuit)

Hand In:

HW 5

Handout:

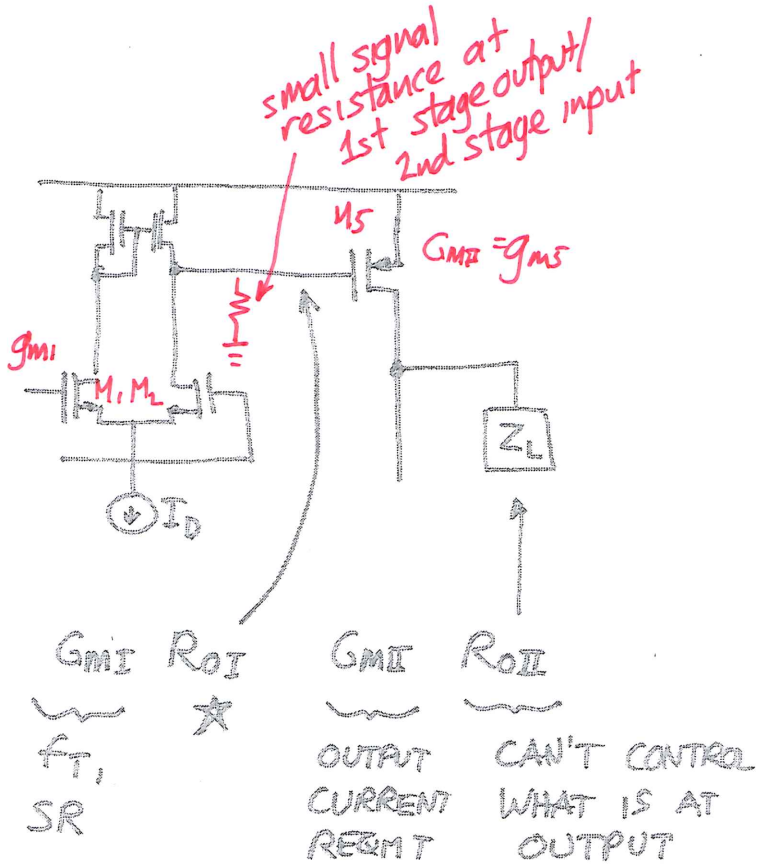
Op-Amp Slides

Cascode Op-Amp

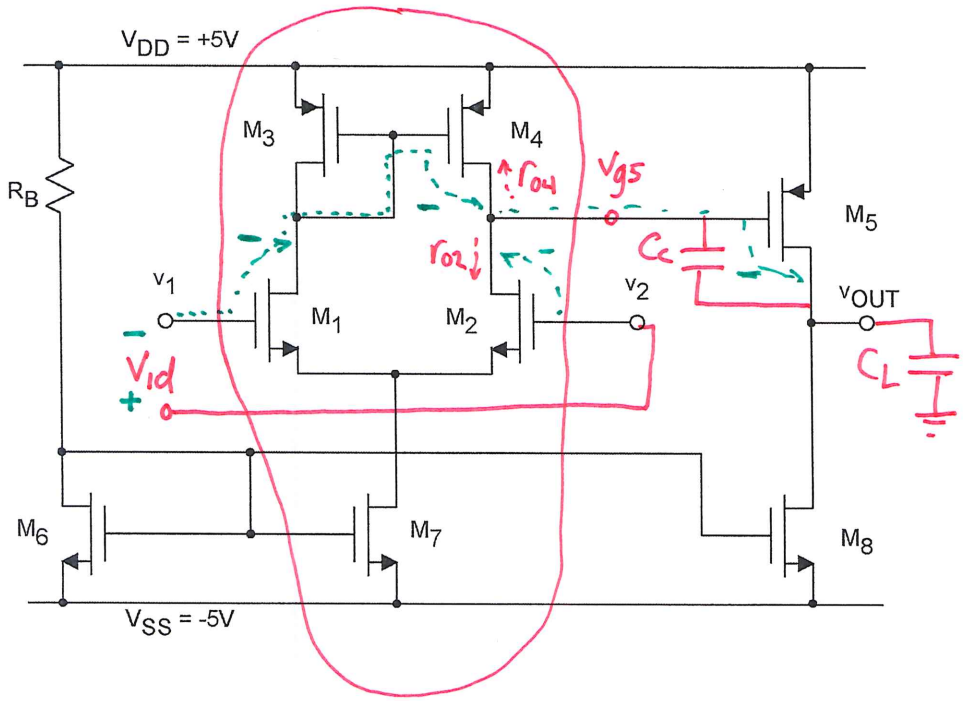
Bandgap Voltage Reference

Principle

Circuit



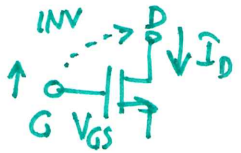
Review: Small signal (ac) model of 2-stage op-amp



IDENTIFY +, - INPUTS: HOW?

FOLLOW SIGNAL PATH FROM INPUT → OUTPUT

COUNT SIGN INVERSIONS

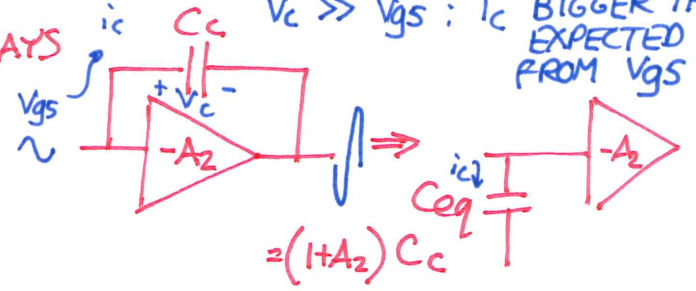


IN THIS CASE $V_1 \Rightarrow V_{OUT}$ 3 INVERSIONS:

V_1 – INPUT

V_2 + INPUT (2 INVERSIONS)

MILLER SAYS



DOMINANT POLE

OUTPUT POLE (NONDOMINANT) [WE HOPE] *

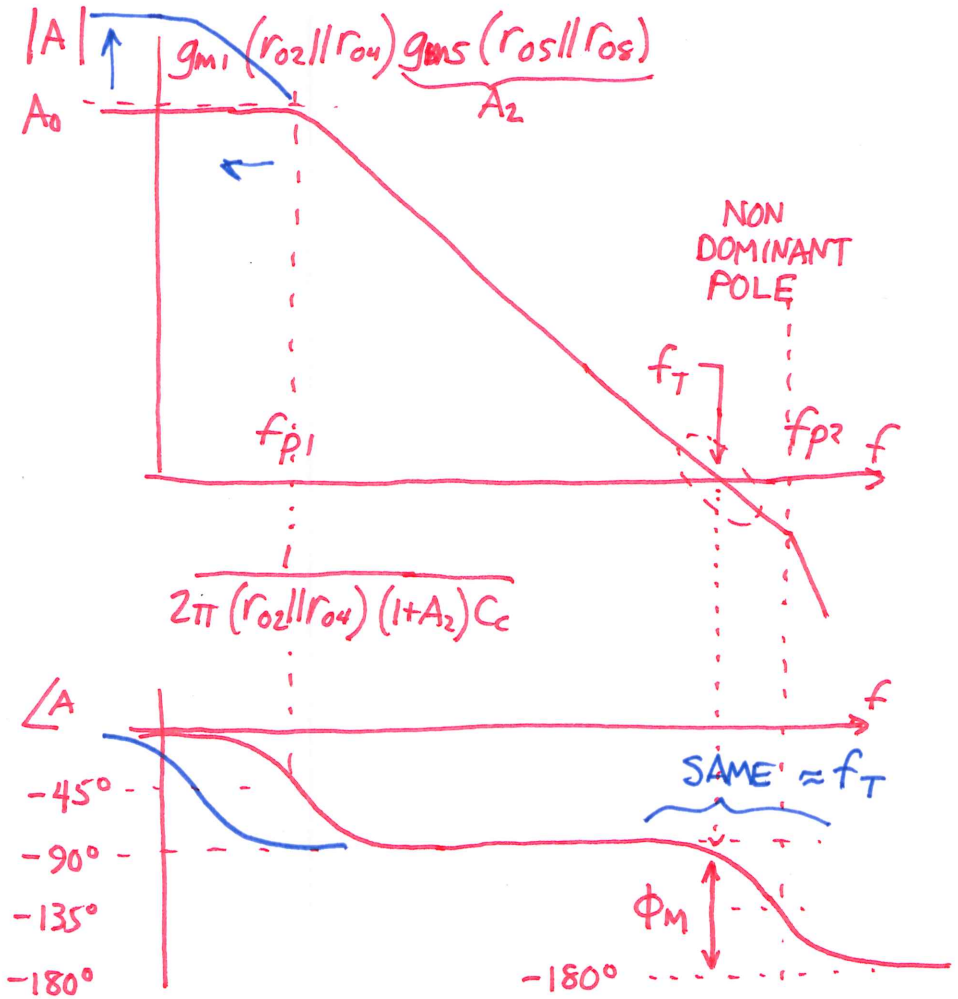
$$\frac{1}{2\pi RC}$$

$$\frac{1}{2\pi (r_{02}||r_{04})\underbrace{(1+A_2)C_c}_{C_{eq}}}$$

$$\frac{1}{2\pi (r_{05}||r_{08})C_L}$$

Complete transfer function, stability plot $(r_{o2}\|r_{o4})\uparrow$

* Increasing node impedance at 1st stage output does not affect phase margin! Separate gain, stability problems



TO APPROXIMATE PHASE NEAR f_T

$$\angle A = \underbrace{-90°}_{\text{1st POLE}} - \tan^{-1}(f/f_{p2})$$

TRY THIS ONE WEIRD TRANSFER FUNCTION TYP

BEHAVIOR OF |A|, ∠A NEAR f_T

$$A(f) = \frac{A_0}{\left(1+j\left(\frac{f}{f_{p1}}\right)\right)\left(1+j\left(\frac{f}{f_{p2}}\right)\right)}$$

MAGNITUDE

$$\frac{A_0}{\sqrt{1+\left(\frac{f}{f_{p1}}\right)^2}\sqrt{1+\left(\frac{f}{f_{p2}}\right)^2}}$$

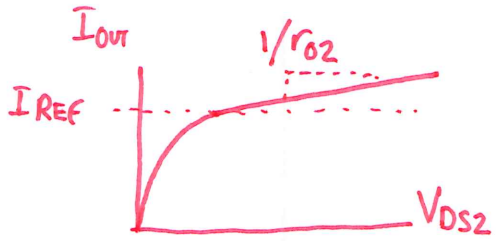
APPROXIMATE: $\frac{f}{f_{p1}} \gg 1$; ≈ 1 FOR $f \ll f_{p2}$

NEAR f_T $|A(f)| \approx \frac{A_0}{\left(\frac{f}{f_{p1}}\right)}$

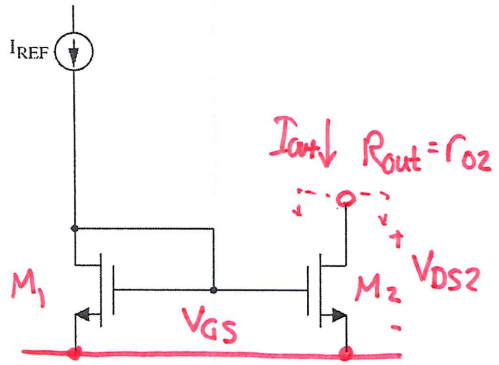
AT f_T $|A(f_T)| = 1$

$$\frac{A_0}{\frac{f_T}{f_{p1}}} = 1 \Rightarrow f_T = A_0 f_{p1}$$

Cascode Current Source Development



$R_{out} = r_{O2} \approx 100k\Omega$



PROBLEM

$$I_{OUT} = I_{D2} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2[1+\lambda V_{DS}]$$

$V_{DS}\uparrow \Rightarrow I_{D2}\uparrow$

HOW TO KEEP I_{D2} FROM CHANGING?

CHANGE L: λ SMALLER ✓ } CAN
SCALE W: MORE AREA × } BE OK

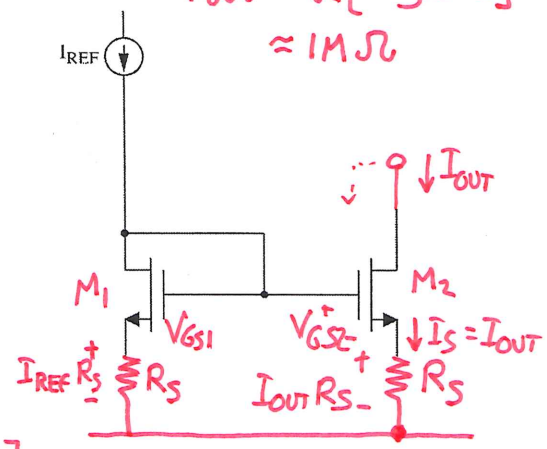
CHANGE V_{GS}

$V_{DS}\uparrow \Rightarrow I_{D2}\uparrow \overset{?}{\Rightarrow} V_{GS}\downarrow$

"SOURCE DEGENERATION"

✓ R_{out} INCREASED
R_S AREA
× HEADROOM REDUCED

$$R_{out} = r_{O2}[1+g_m R_S]$$
$$\approx 1M\Omega$$



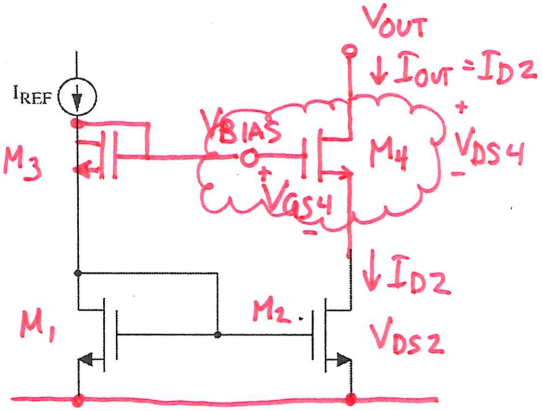
KVL LOOP

$$I_{REF}R_S + V_{GS1} - V_{GS2} - I_{OUT}R_S = 0$$

$$V_{GS2} = V_{GS1} - \underbrace{(I_{OUT}-I_{REF})R_S}_{\text{NEGATIVE FEEDBACK!}}$$

$I_{OUT}\uparrow \Rightarrow V_{GS2}\downarrow$

$$R_{out} = r_{O4}(1+g_{m4}r_{O2})$$
$$\approx 10M\Omega \quad \surd\surd$$
HEADROOM ××



PROBLEM

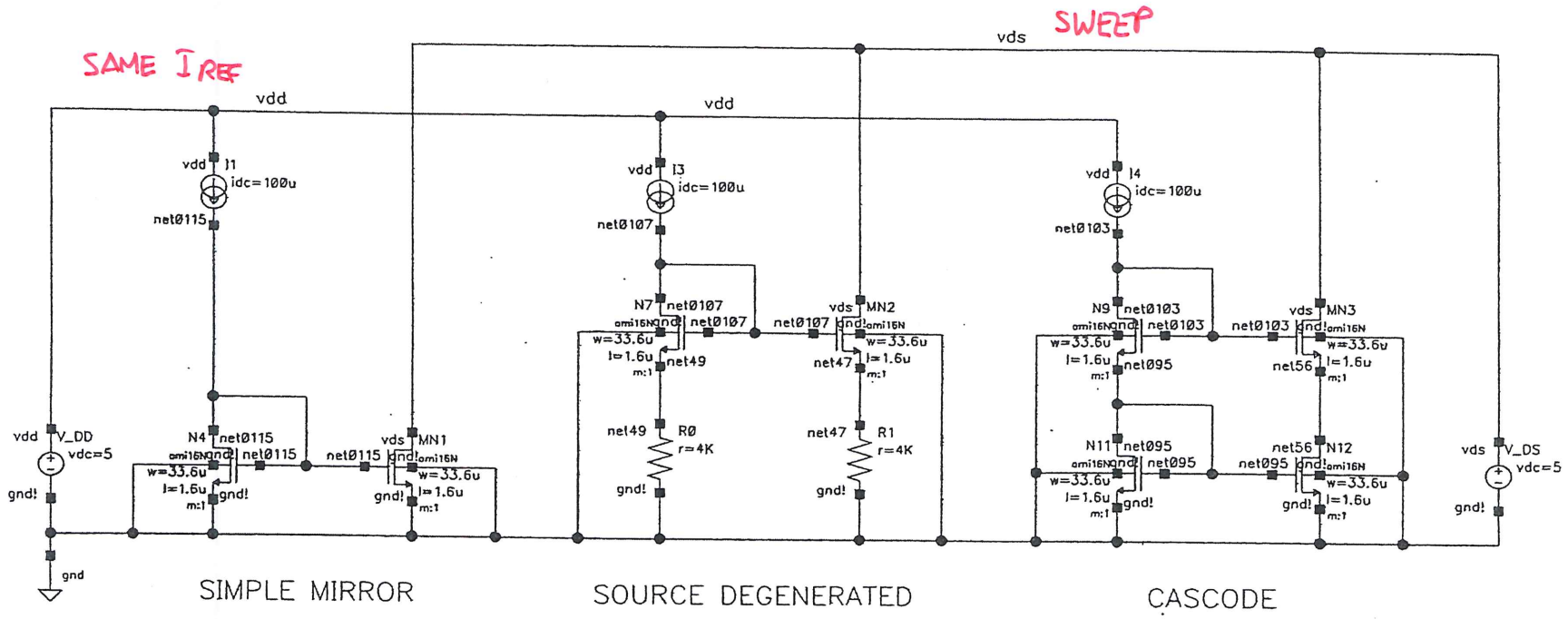
V_{OUT} CHANGED V_{DS2}
$\Rightarrow$ CHANGED I_{D2}
MAGIC: PASSES I_{D2} THRU BUT KEEPS V_{DS2} CONSTANT!?

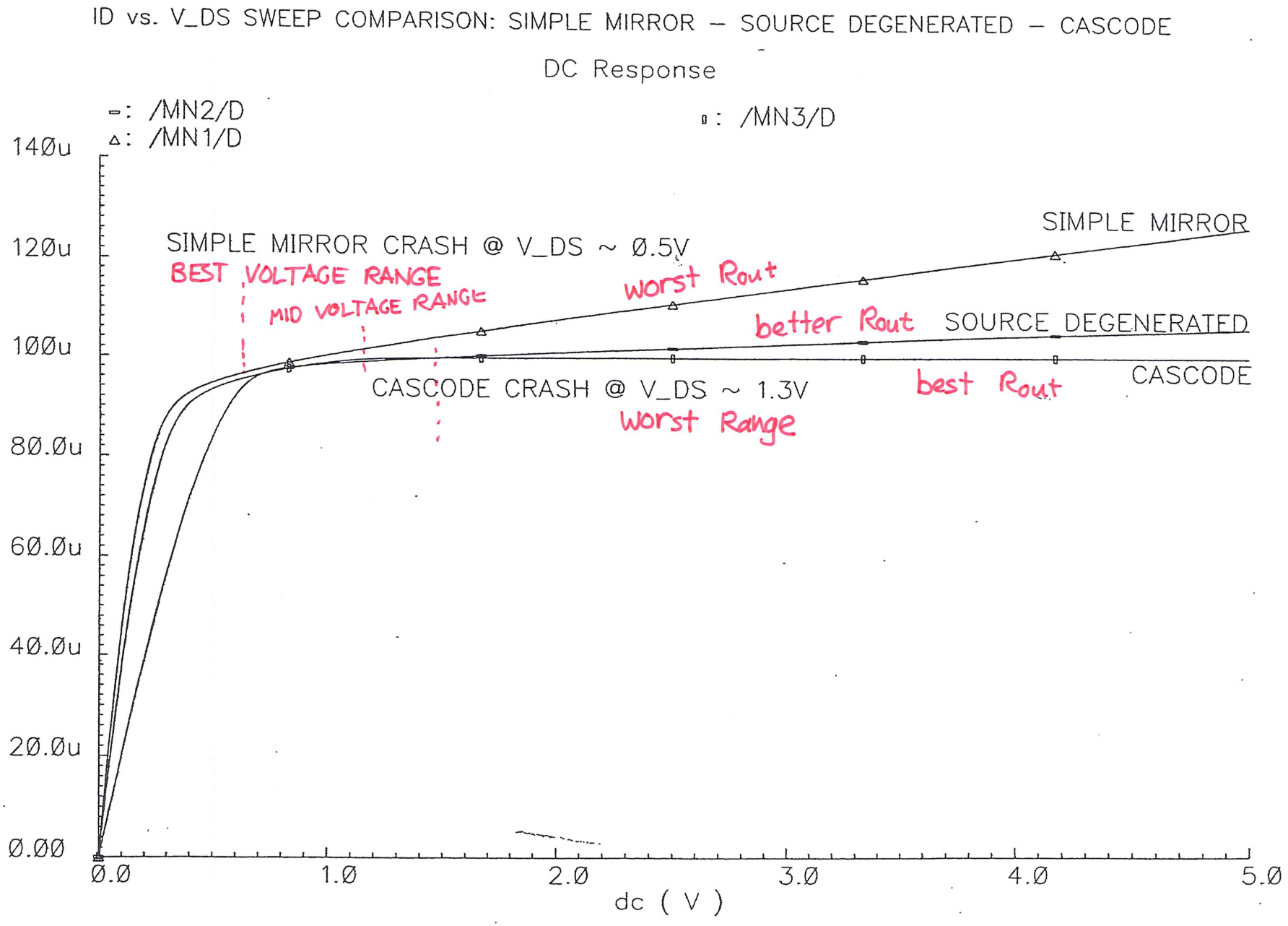
M_4: $I_D = I_S$

VOLTAGE? $V_{DS2} = V_{BIAS} - \underbrace{V_{GS4}}_{\sim\text{CONSTANT}}$

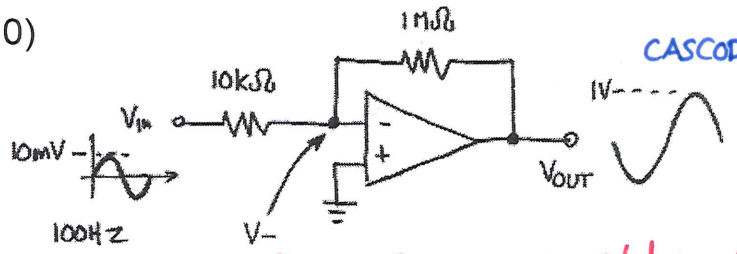
M_4: "CASCODE"

Current source comparison: Simulation



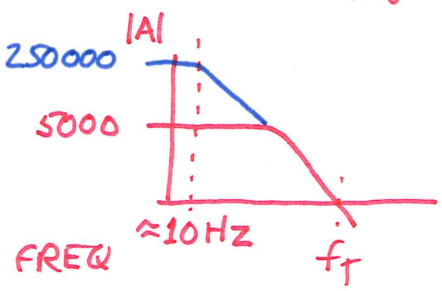

ID vs. V_DS SWEEP COMPARISON: SIMPLE MIRROR – SOURCE DEGENERATED – CASCODE
DC Response
-: /MN2/D
△: /MN1/D
▯: /MN3/D
140u
120u
100u
80.0u
60.0u
40.0u
20.0u
0.00
0.0
1.0
2.0
3.0
4.0
5.0
dc (V)
SIMPLE MIRROR CRASH @ V_DS ~ 0.5V
BEST VOLTAGE RANGE
MID VOLTAGE RANGE
worst Rout
SIMPLE MIRROR
better Rout
SOURCE DEGENERATED
CASCODE CRASH @ V_DS ~ 1.3V
worst Range
best Rout
CASCODE

Cascode Op-Amp (Optional Lab 10)

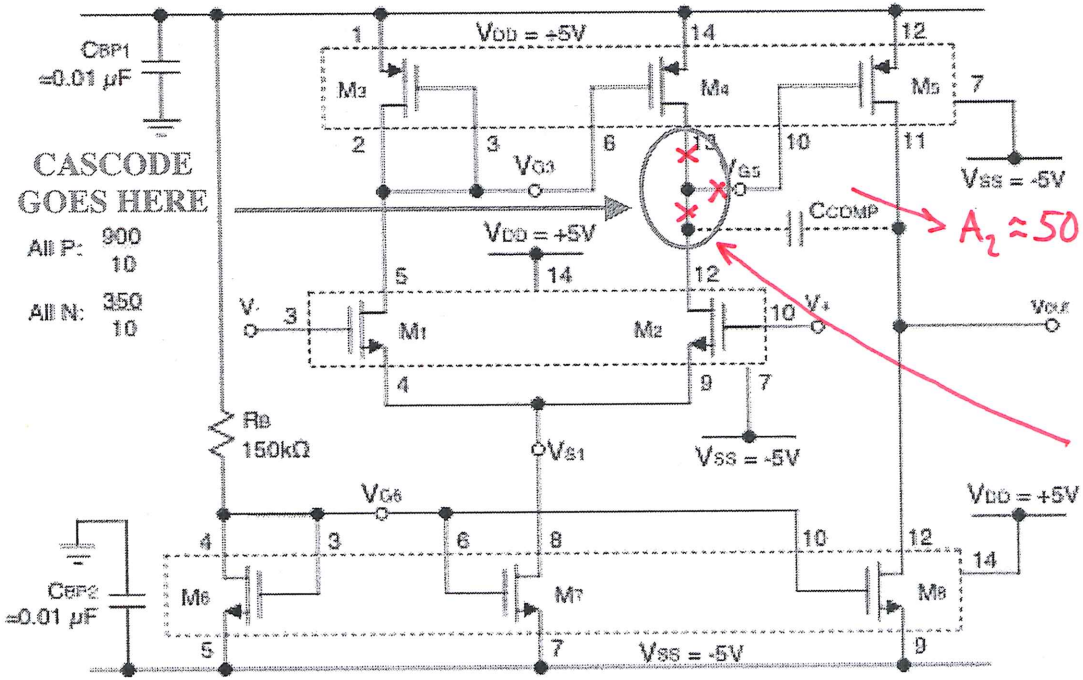


ORIGINAL 2 STAGE $A_0 = 5000$

CASCODE



CRANK UP TO ~ 1mV/div, LOW FREQ



5V

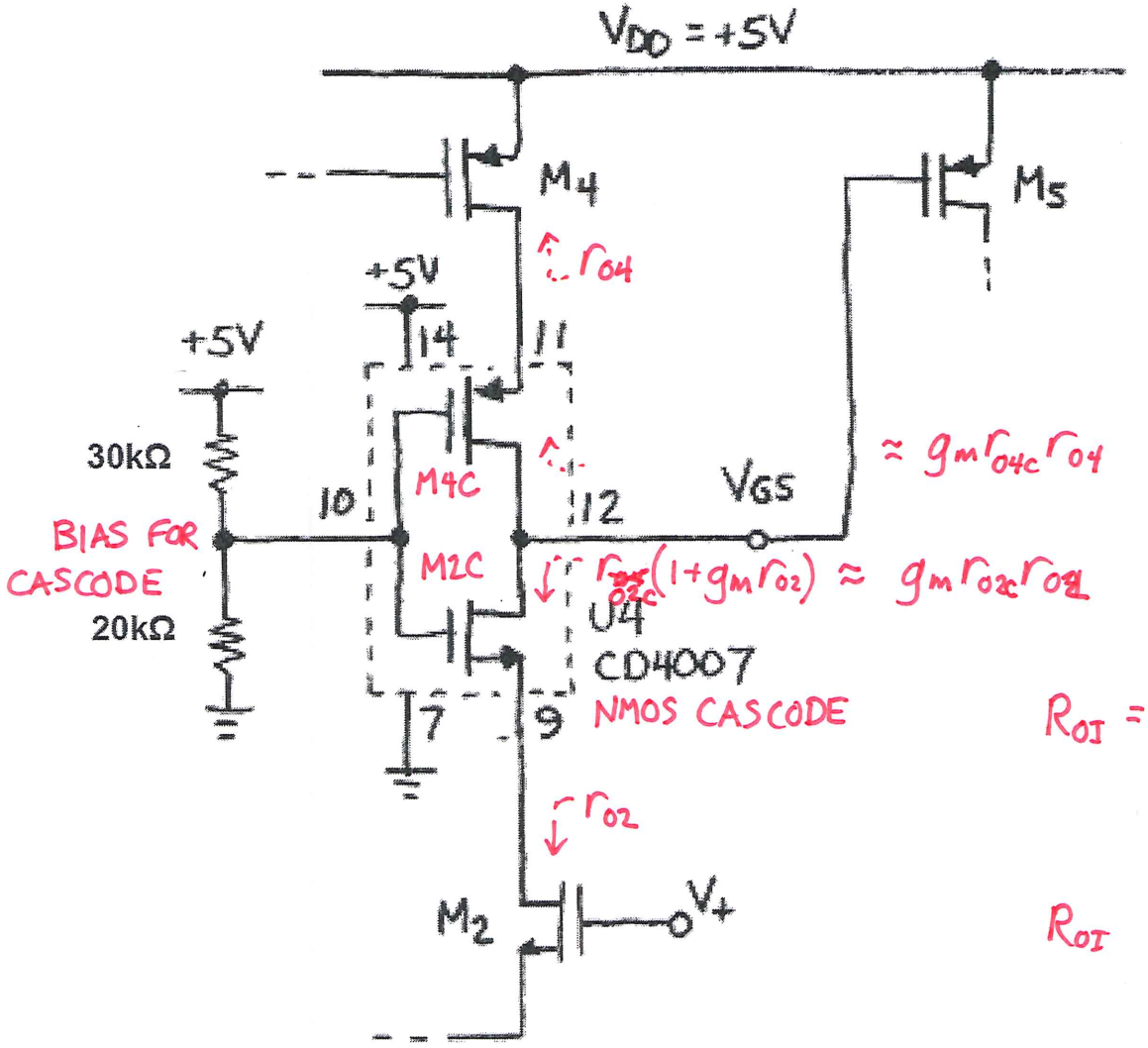
WHAT IS SIGNAL SWING HERE?

$V_{OUT} = 5V$

$V_{GS} = \frac{5V}{50} = 0.1V$

Figure 9.1

To cascode the internal node, you'll need a fourth CD4007 chip. Connect it as shown here:



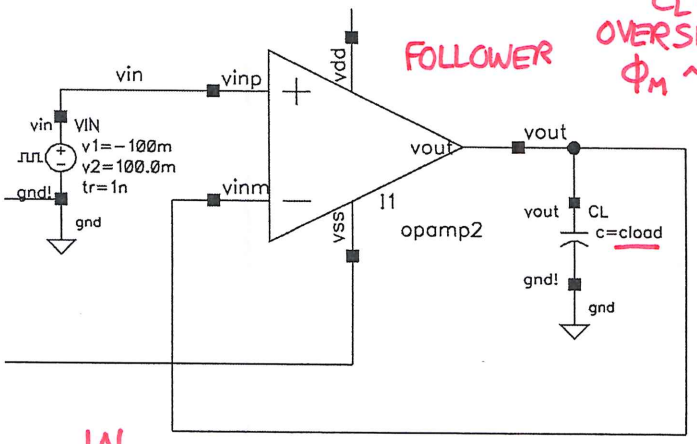
$R_{OI} = r_{O2c}\, r_{O2}\, g_m \,\|\, r_{O4c}\, r_{O4}\, g_m$

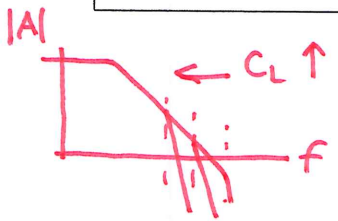
≈ EQUAL

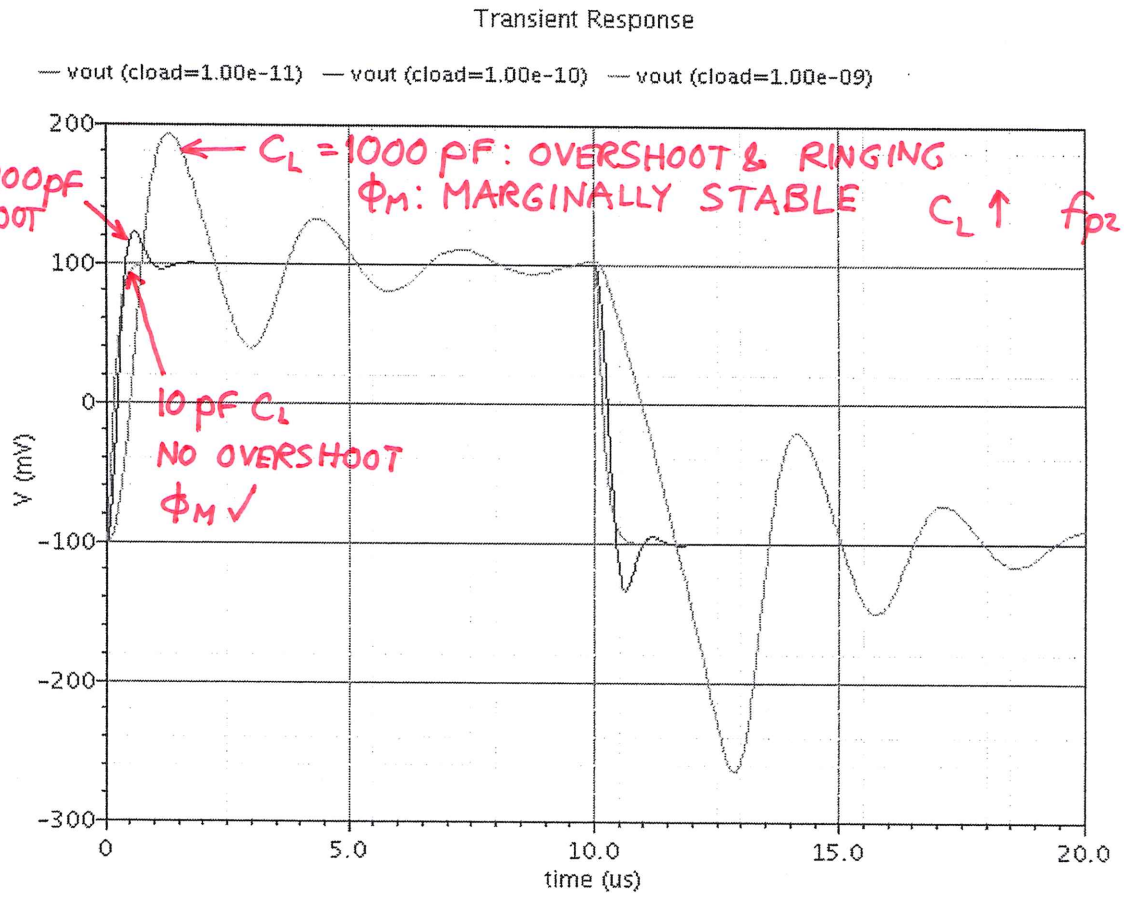
R_{OI} INCREASED BY FACTOR OF $\sim g_m r$

50

2-Stage Op-Amp Phase Margin vs. C_{LOAD}

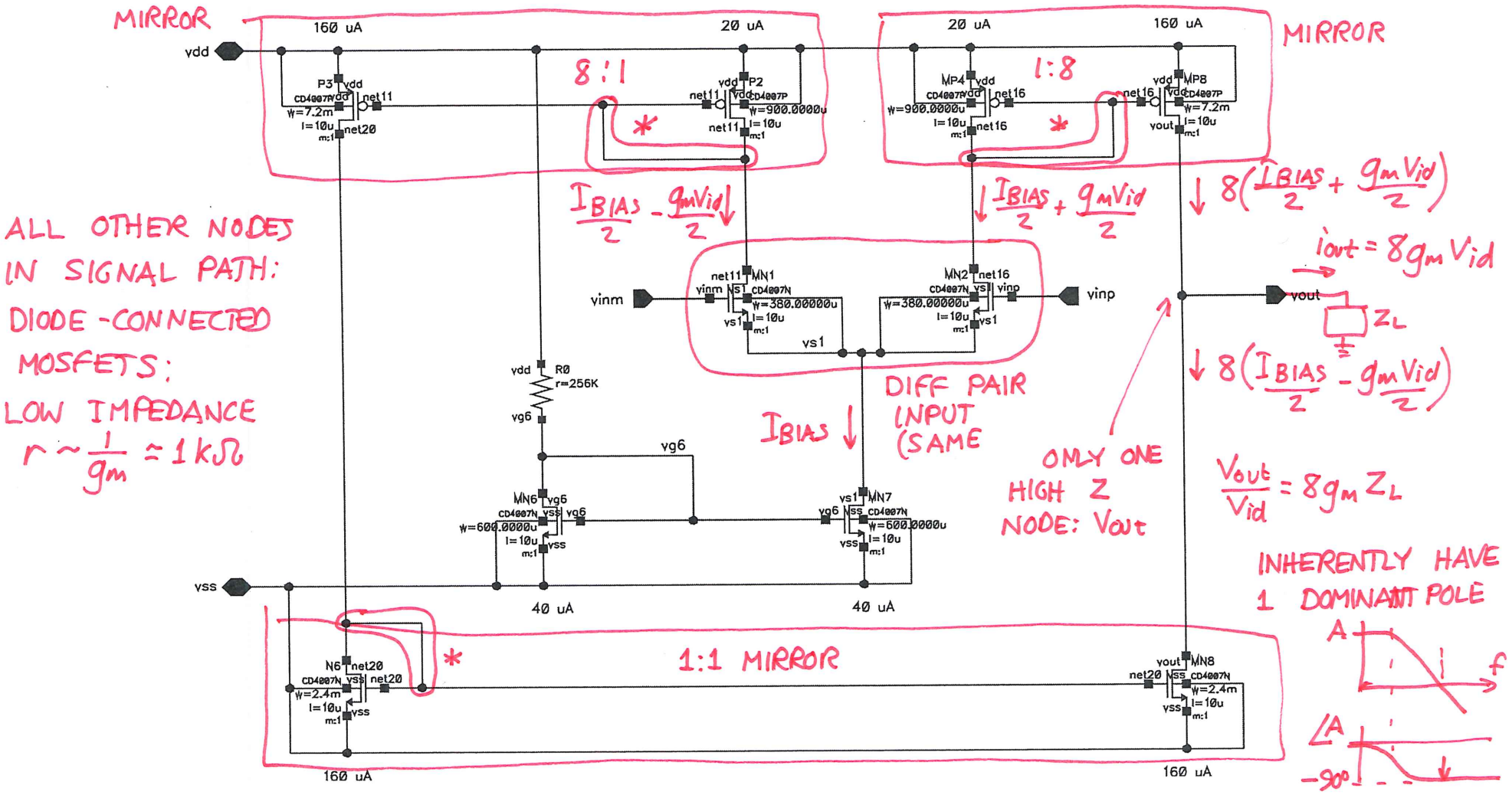






- C_{LOAD} = 10pF, 100pF, 1000pF
- Phase margin ϕ_M degrades as C_{LOAD} increases

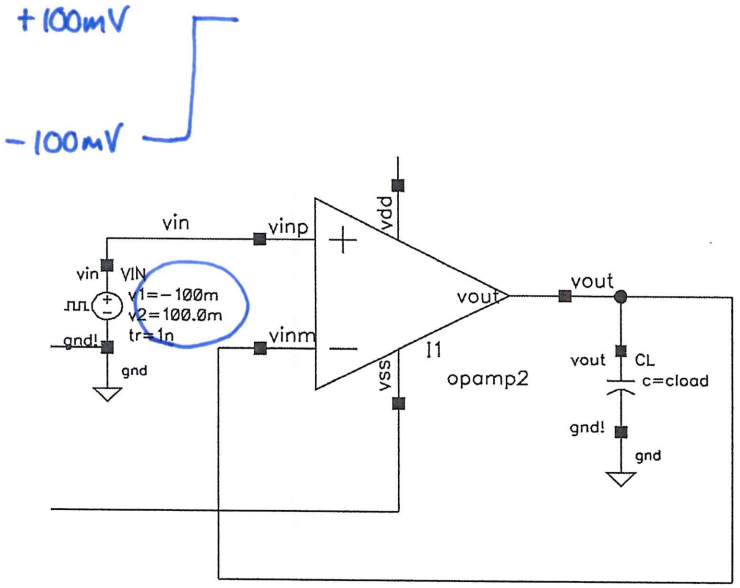
1-Stage ("gm-C" "transconductor") Op-Amp

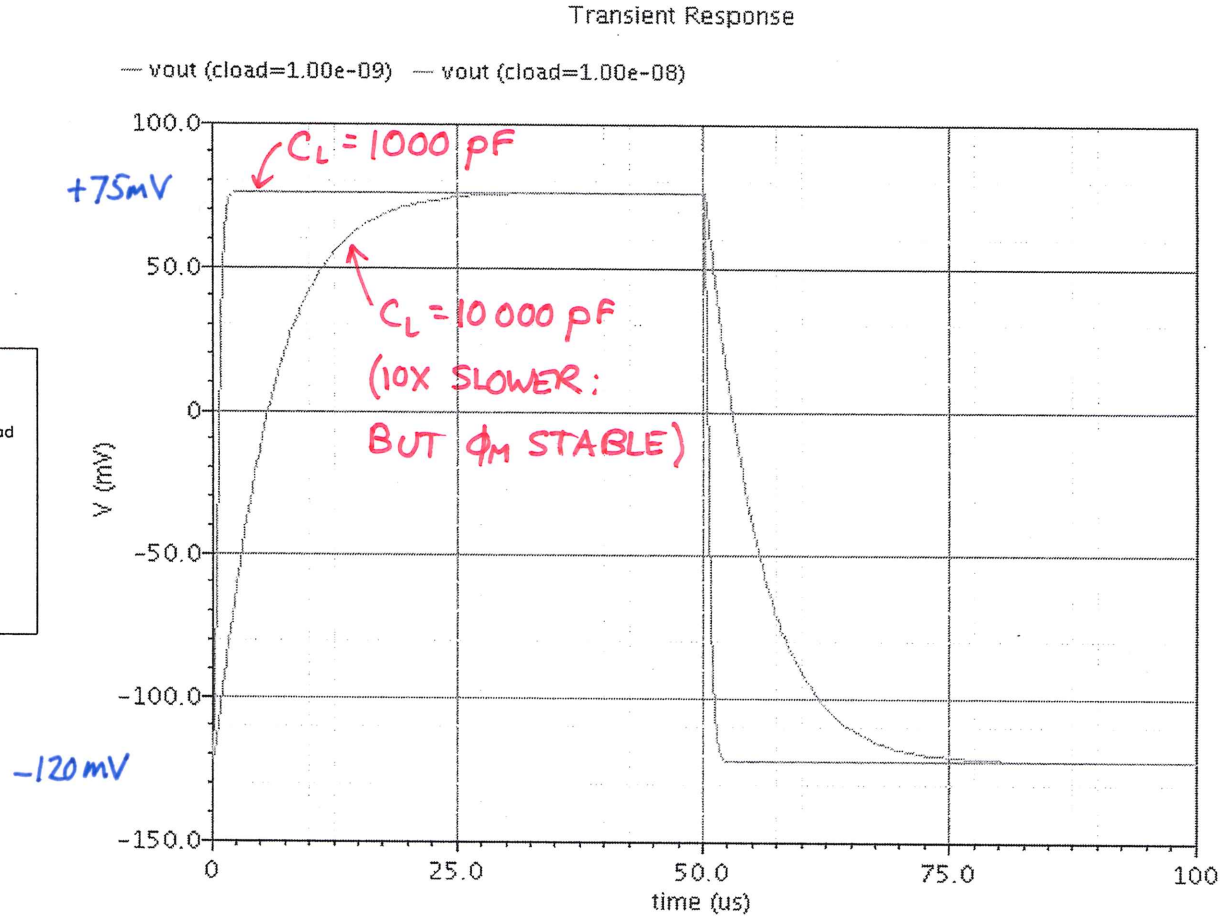


- Only one high impedance node: C_{LOAD} compensates

$\phi_M = 90°$

1-Stage ("gm-C" "transconductor") Op-Amp

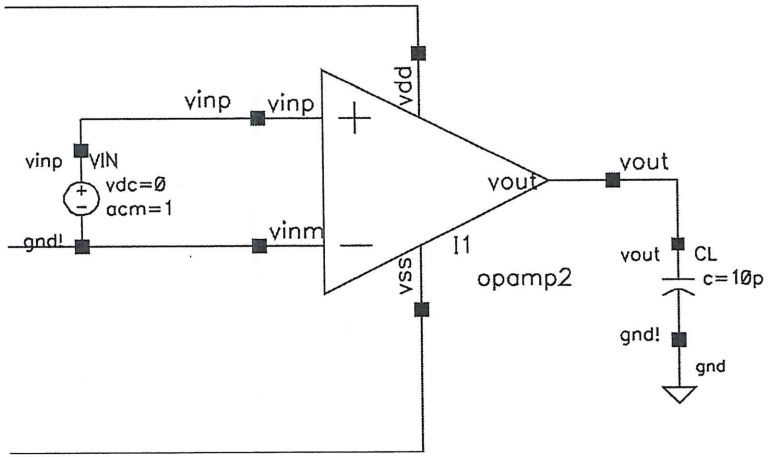




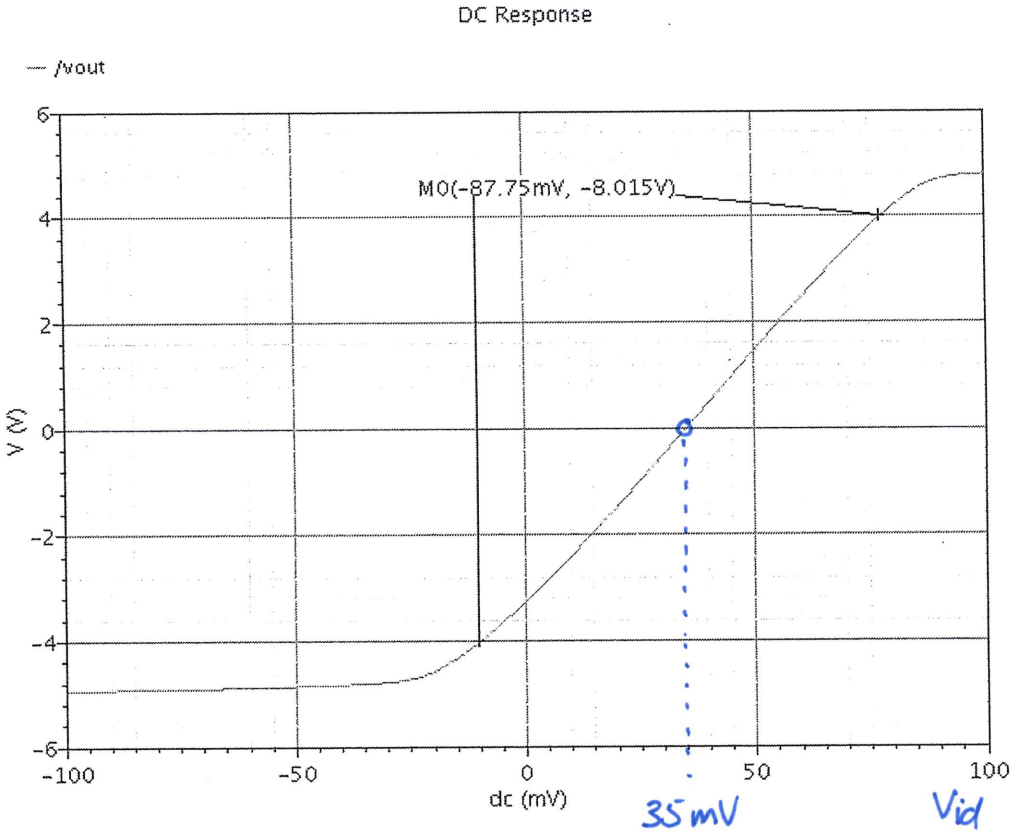
- C_{LOAD} = 1000pF, 10000pF: ϕ_M same as C_{LOAD} ⇧
- Unity gain frequency f_T worse, but always stable

1-Stage Problem

OPEN LOOP DC $V_{in} \rightarrow V_{out}$

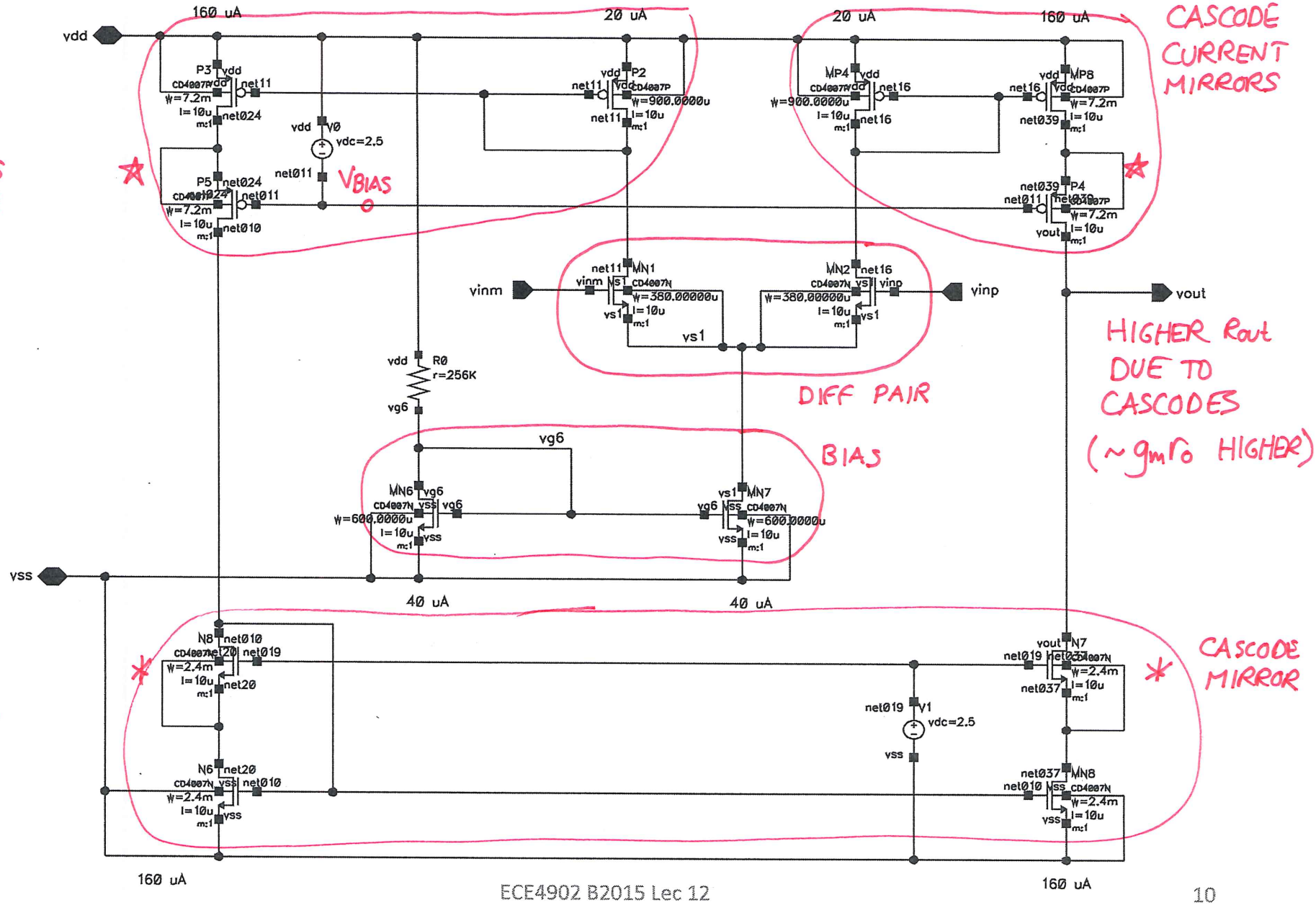


Vout



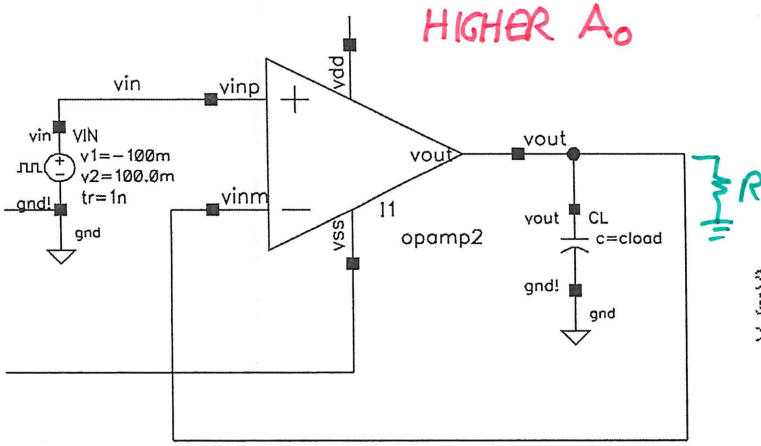
- Lousy DC gain ≈ 90 (39 dB) NOT ENOUGH FOR MOST OP-AMP APPLICATIONS
- Solution: Add cascode to high impedance node

1-Stage with Cascodes

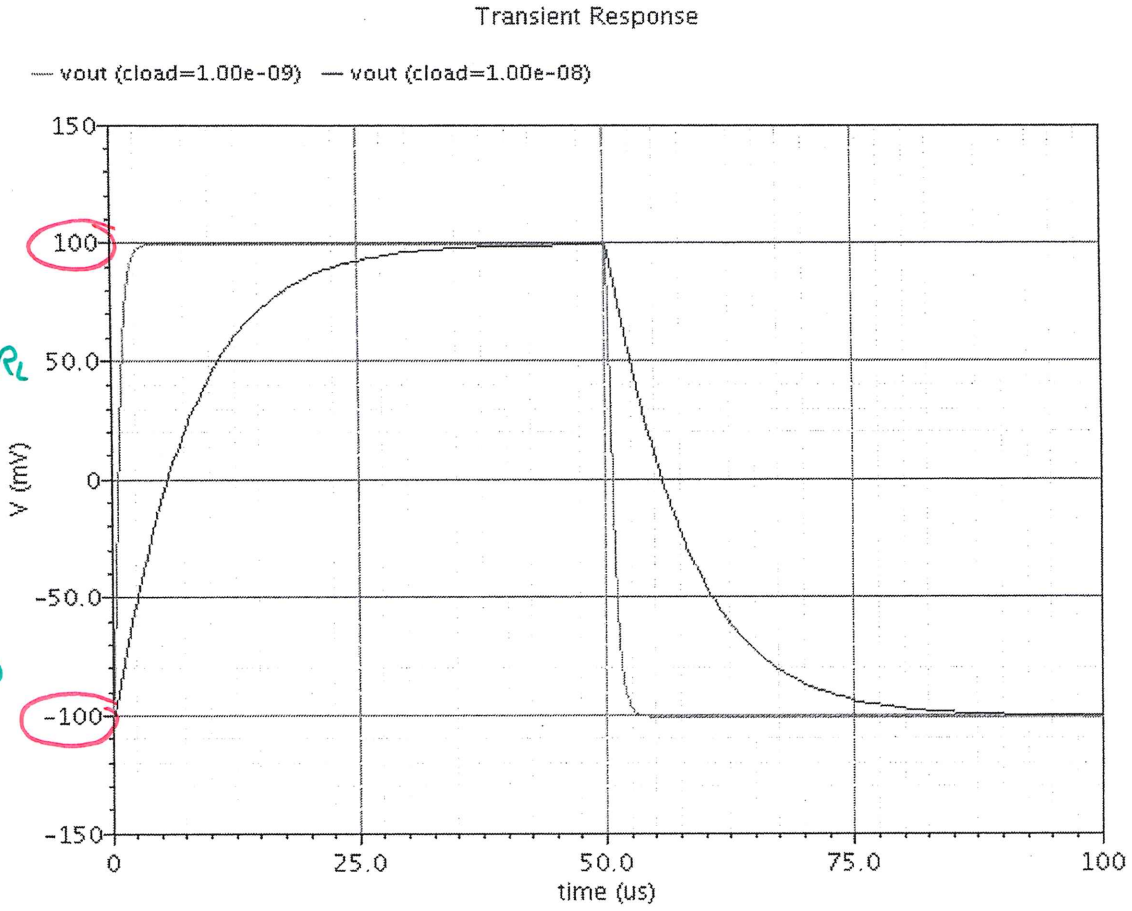


1-Stage with Cascodes

MORE ACCURATE DC PERFORMANCE DUE TO HIGHER A_o



ONLY WORKS WITH CAPACITIVE LOAD
IF R_L: NEED LOW OUTPUT Z OUTPUT STAGE



- C_{LOAD} = 1000pF, 10000pF: ϕ_M same as C_{LOAD} ⇧ } DYNAMIC SAME
- Unity gain frequency f_T worse, but always stable

Bandgap Voltage Reference (Optional Lab 11)

Motivation: DC Bias

I_{BIAS}: SLEW RATE (I_{SS})

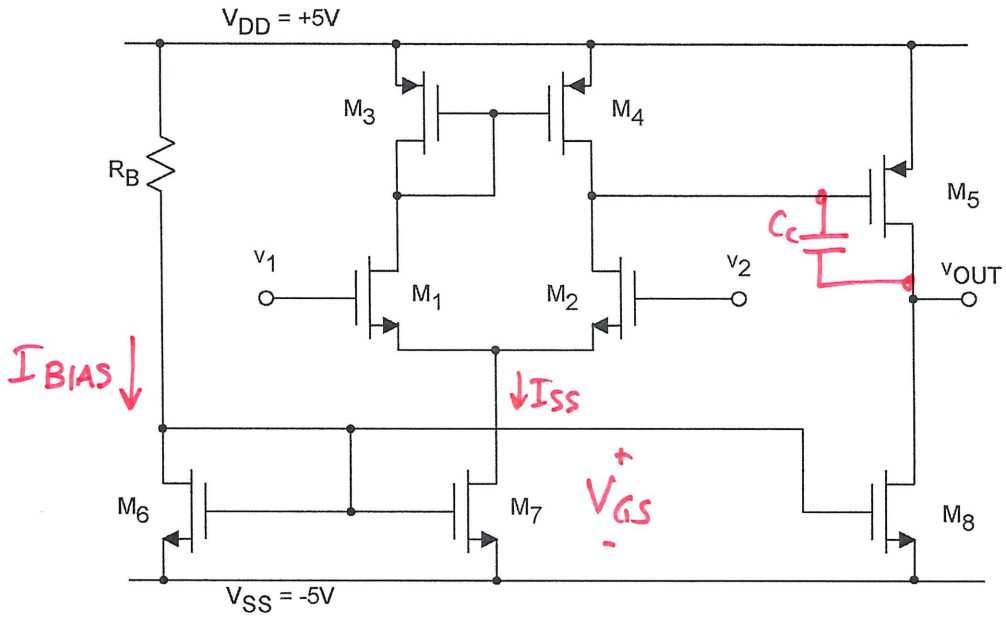
↳ g_{m1} INPUT STAGE

$$f_T = \frac{g_{m1}}{2\pi C_C}$$

$$I_{BIAS} = \frac{(V_{DD} - V_{SS}) - V_{GS}}{R_{BIAS}}$$

COULD CHANGE!? SUPPLY!

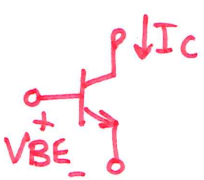
TEMPERATURE CHANGE



⇒ WANT I_{SS}, SR, f_T, ... INSENSITIVE TO SUPPLY, TEMP VARIATIONS!

Bandgap Principle

BJT



$I_S \propto$ EMITTER AREA

DOUBLES EVERY 10°C

$I_C = I_S e^{(V_{BE}/V_T)}$

SCALE CURRENT

BOLTZMANN'S CONSTANT

"THERMAL VOLTAGE" $\frac{kT}{q}$, k: BOLTZMANN'S CONSTANT, T: ABS TEMP, q: e^- CHARGE

≈26mV AT T=300K

$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$

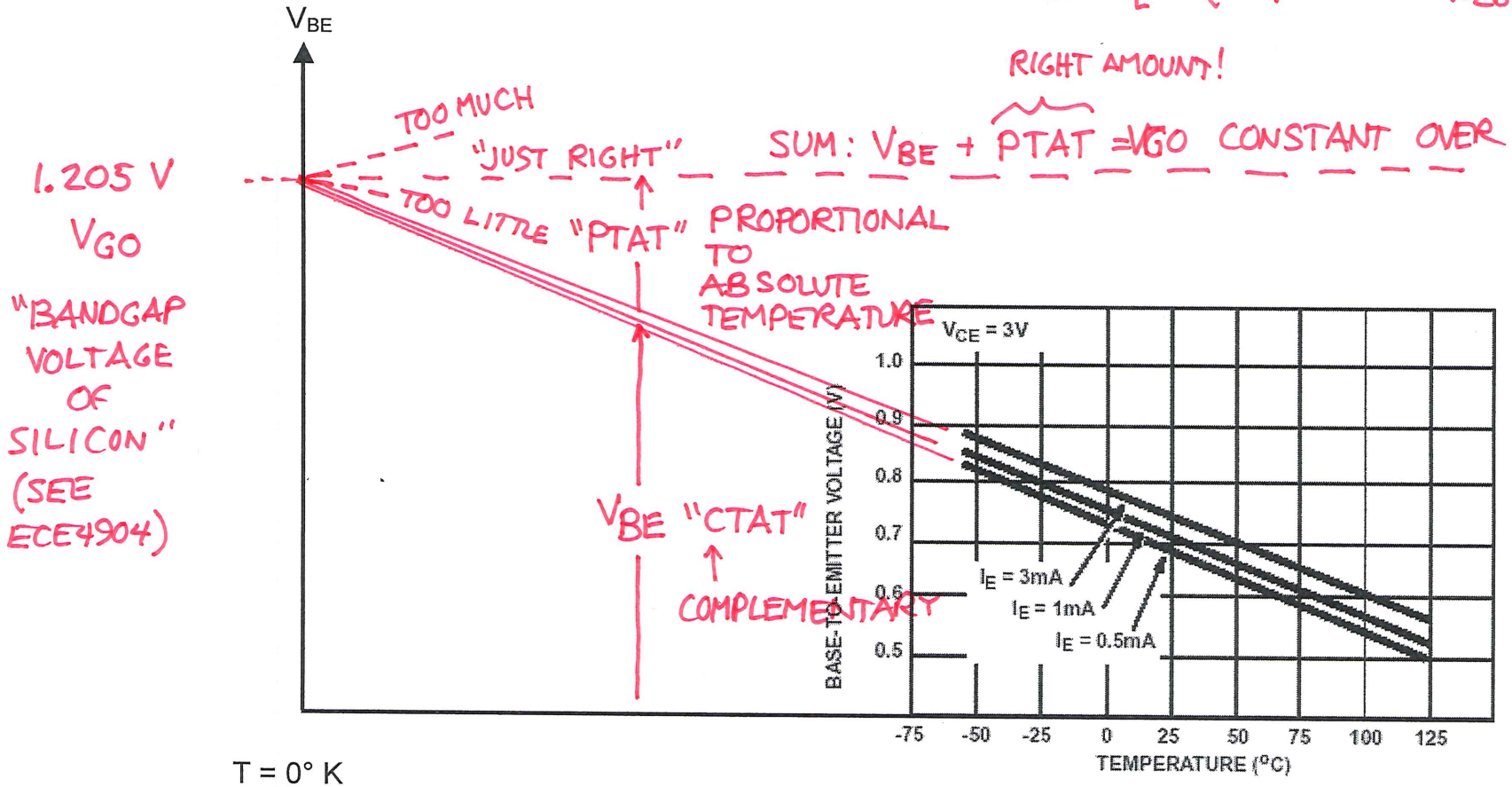
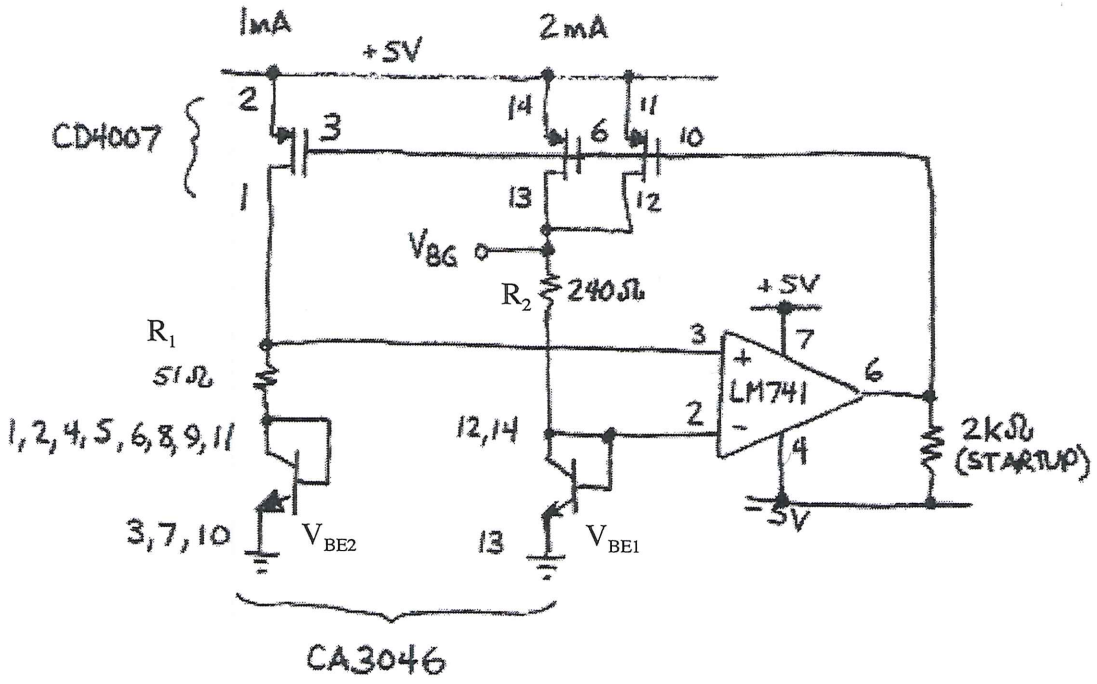


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

BANDGAP VOLTAGE REFERENCE

Here's the bandgap circuit covered in lecture:



The CA3046 is a 5 NPN transistor array. Its data sheet is available on the course website.