ECE4902 Lecture 13

Finish Bandgap Voltage Reference

Phase Locked Loop
- Loop Components
- FM Demodulation
- Clock Frequency Multiplication

Matching Issues
- Differential Pair
- Current Mirror

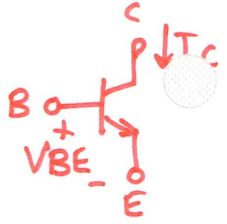
MOS vs. BJT Comparison
- Short Channel Effects

Course Evaluations

Handouts:
Offset Voltage Math
MOS vs. BJT

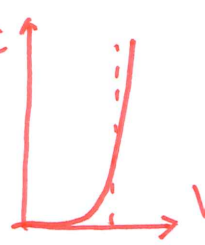
Reminder:
All Labs / Late HW must be handed in by 5pm Thursday December 17th!!!

BJT



$I_S \propto$ EMITTER AREA

DOUBLES EVERY 10°C



$I_C = I_S e^{(V_{BE}/V_T)}$

SCALE CURRENT

BOLTZMANN'S CONSTANT

"THERMAL VOLTAGE" $\frac{kT}{q}$, ABS TEMP, e^- CHARGE

$\approx 26mV$ AT T=300K

$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$

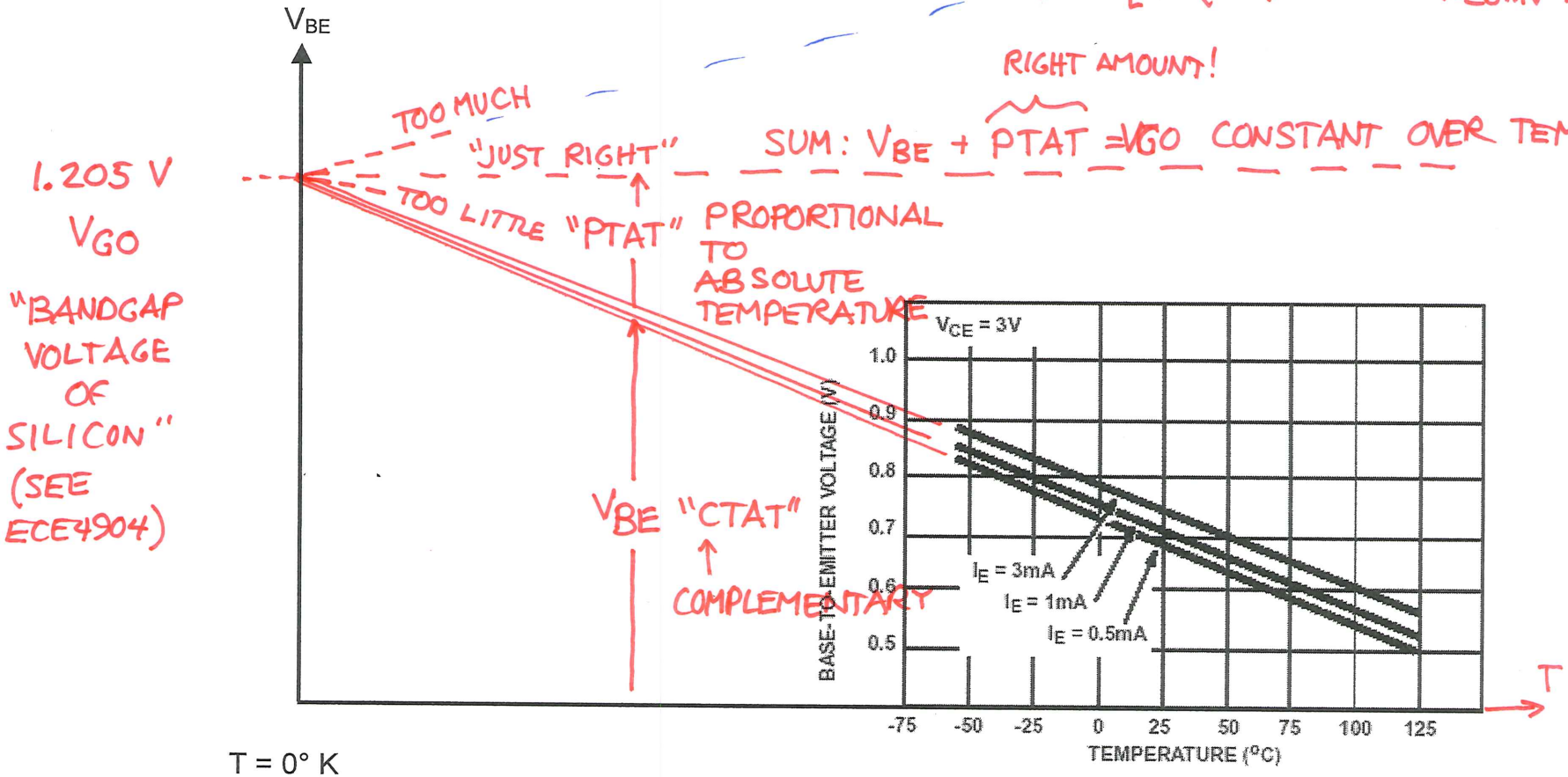
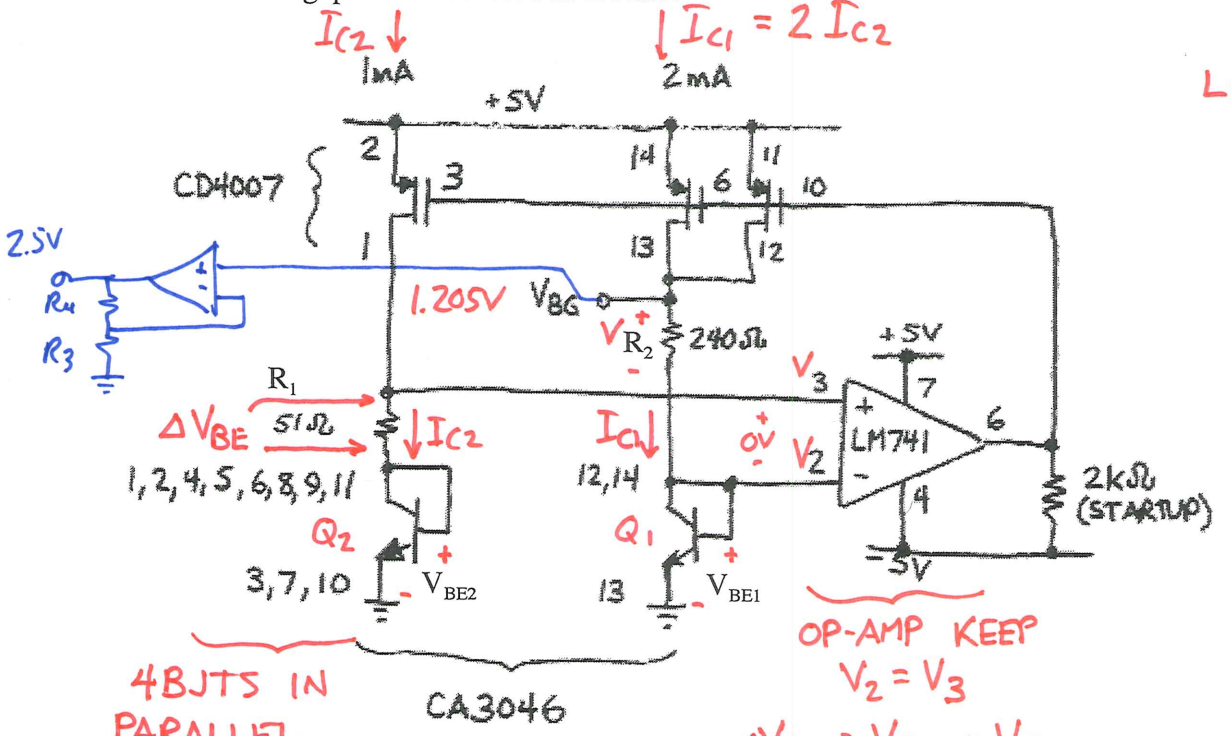


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

BANDGAP VOLTAGE REFERENCE

Here's the bandgap circuit covered in lecture:



The CA3046 is a 5 NPN transistor array. Its data sheet is available on the course website.

→ Q2 HAS 4X EMITTER AREA RELATIVE TO Q1 ⇒ $I_{S2} = 4I_{S1}$ (GEOMETRY)

CURRENT: $I_{C2} = \frac{\Delta V_{BE}}{R_1} \Rightarrow I_{C1} = \frac{2\Delta V_{BE}}{R_1} \Rightarrow V_{R_2} = I_{C1}R_2 = \frac{2R_2}{R_1}\Delta V_{BE}$

Q_1, Q_2 BJTS:

$$V_{BE2} = \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{S2}}\right) \qquad V_{BE1} = \frac{kT}{q}\ln\left(\frac{I_{C1}}{I_{S1}}\right)$$

LOOK AT ΔV_{BE}

$$\Delta V_{BE} = \frac{kT}{q}\left[\ln\left(\frac{I_{C1}}{I_{S1}}\right) - \ln\left(\frac{I_{C2}}{I_{S2}}\right)\right]$$

$\ln x - \ln y = \ln\left(\frac{x}{y}\right)$

$$\Delta V_{BE} = \frac{kT}{q}\ln\left[\frac{I_{C1}}{I_{C2}}\,\frac{I_{S2}}{I_{S1}}\right]$$

MIRROR: $\frac{I_{C1}}{I_{C2}} = 2$; $\frac{I_{S2}}{I_{S1}} = 4$ EMITTER AREAS

$$\Delta V_{BE} = \frac{kT}{q}\ln(8) = \left[\frac{k}{q}\ln(8)\right]T$$

ΔV_{BE} IS PTAT!

KVL TO V_{BG}

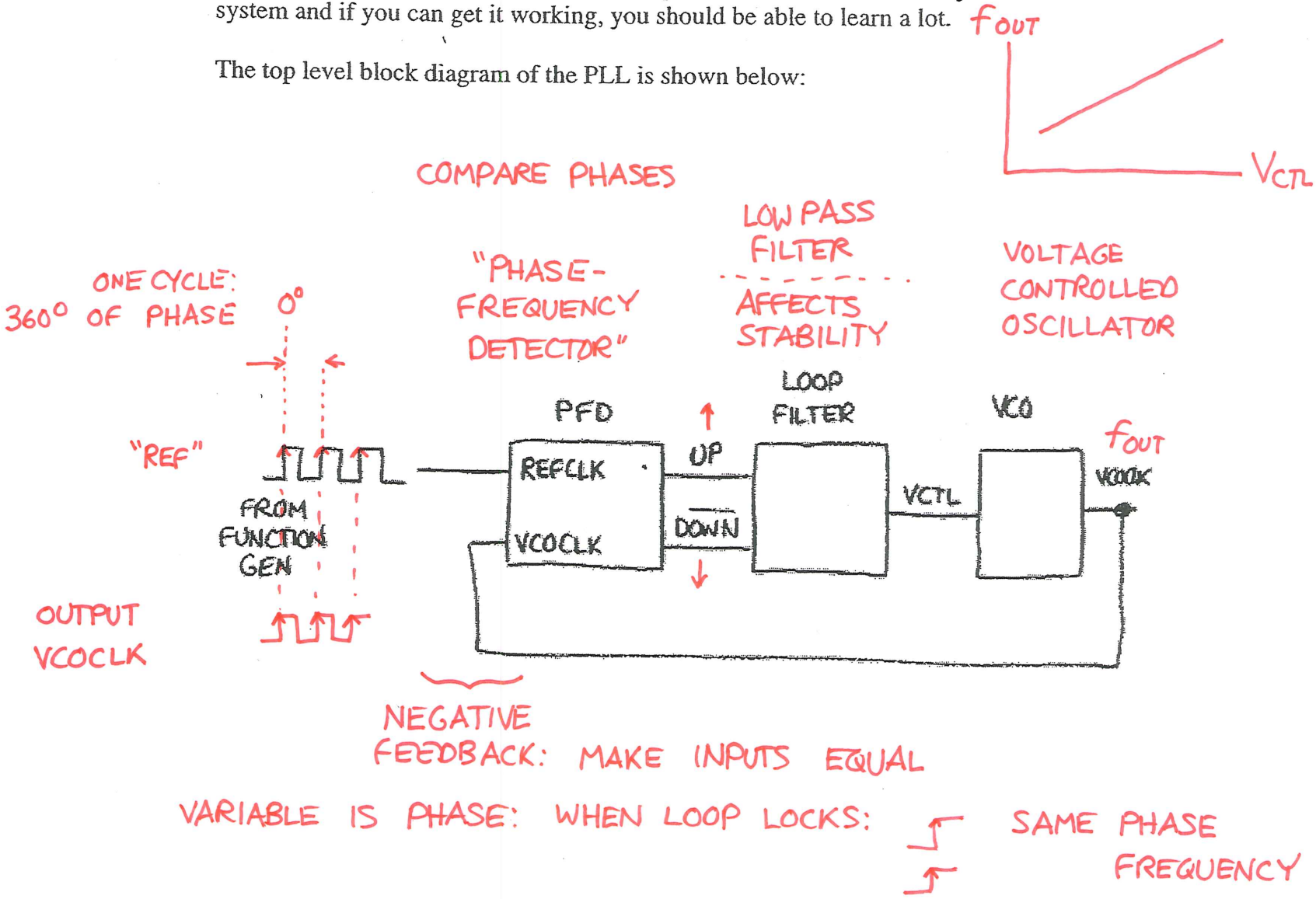
$$V_{BG} = V_{BE1} + \left(\frac{2R_2}{R_1}\right)\Delta V_{BE}$$

ADJUST TO GET $V_{BG} = 1.205$V

PLL

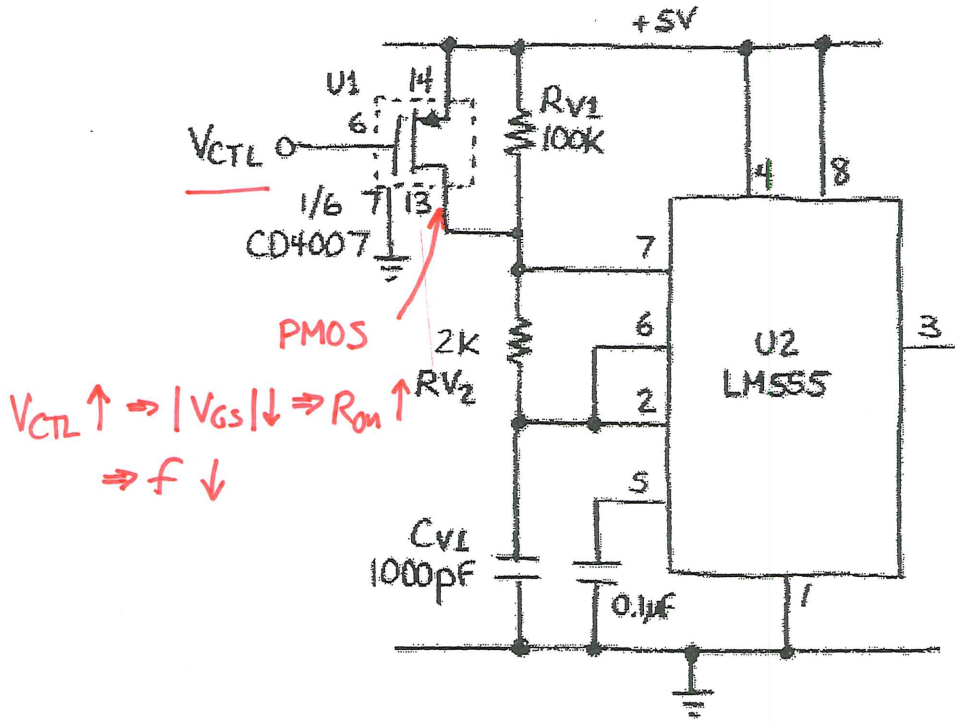
This is the most complicated of the three optional labs - but is definitely the coolest system and if you can get it working, you should be able to learn a lot.

The top level block diagram of the PLL is shown below:



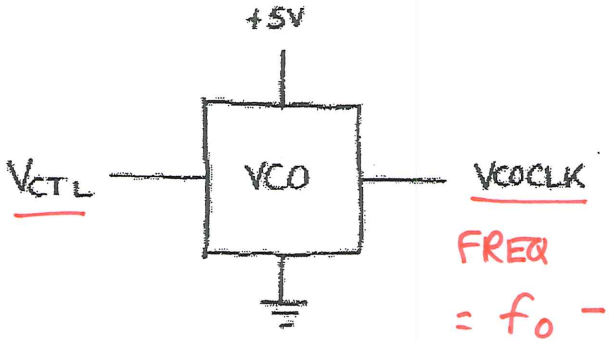
BUILDING THE SYSTEM

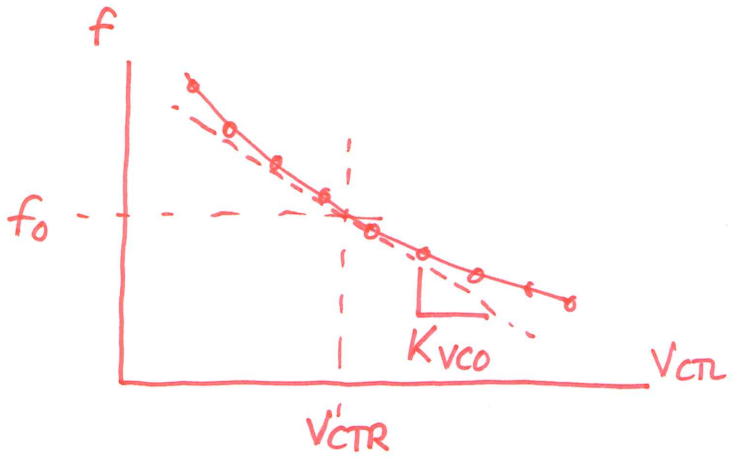
The first step is to build the VCO block by itself and verify its operation:



$V_{CTL} \uparrow \Rightarrow |V_{GS}| \downarrow \Rightarrow R_{on} \uparrow \Rightarrow f \downarrow$

$f \propto \frac{1}{RC}$ (R_A, R_B)

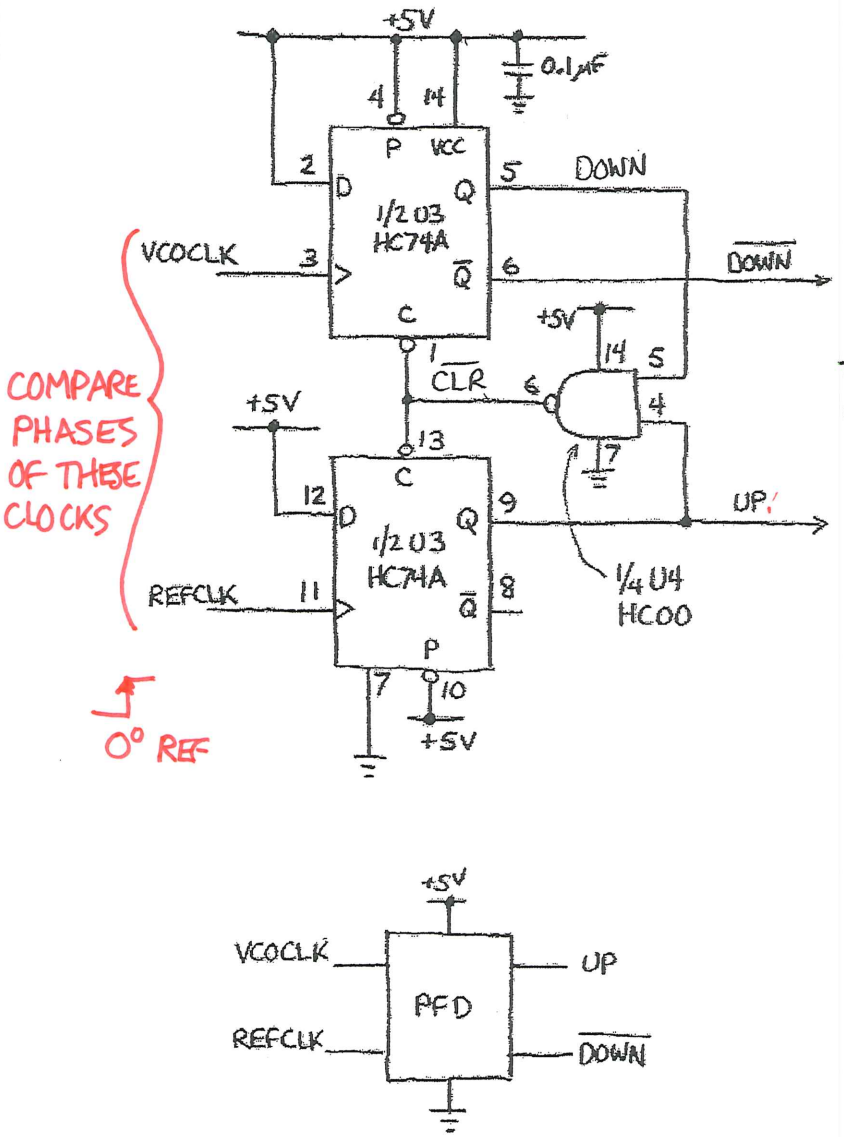


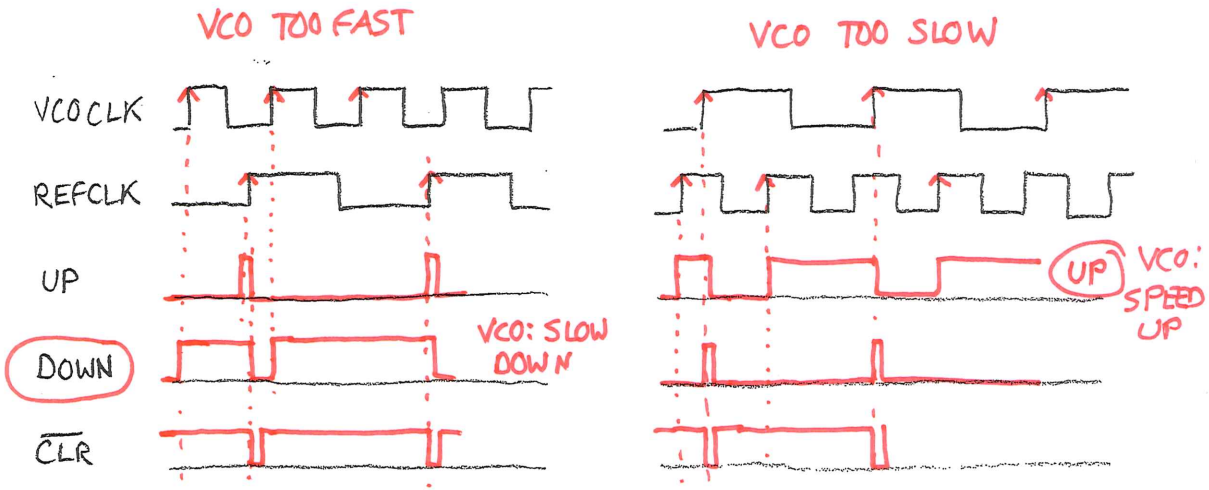


FREQ $= f_0 - K_{VCO}(V_{CTL} - V_{CTR})$

"CENTER FREQUENCY" f_0; K_{VCO} in $\frac{Hz}{V}$

Next build the PFD:

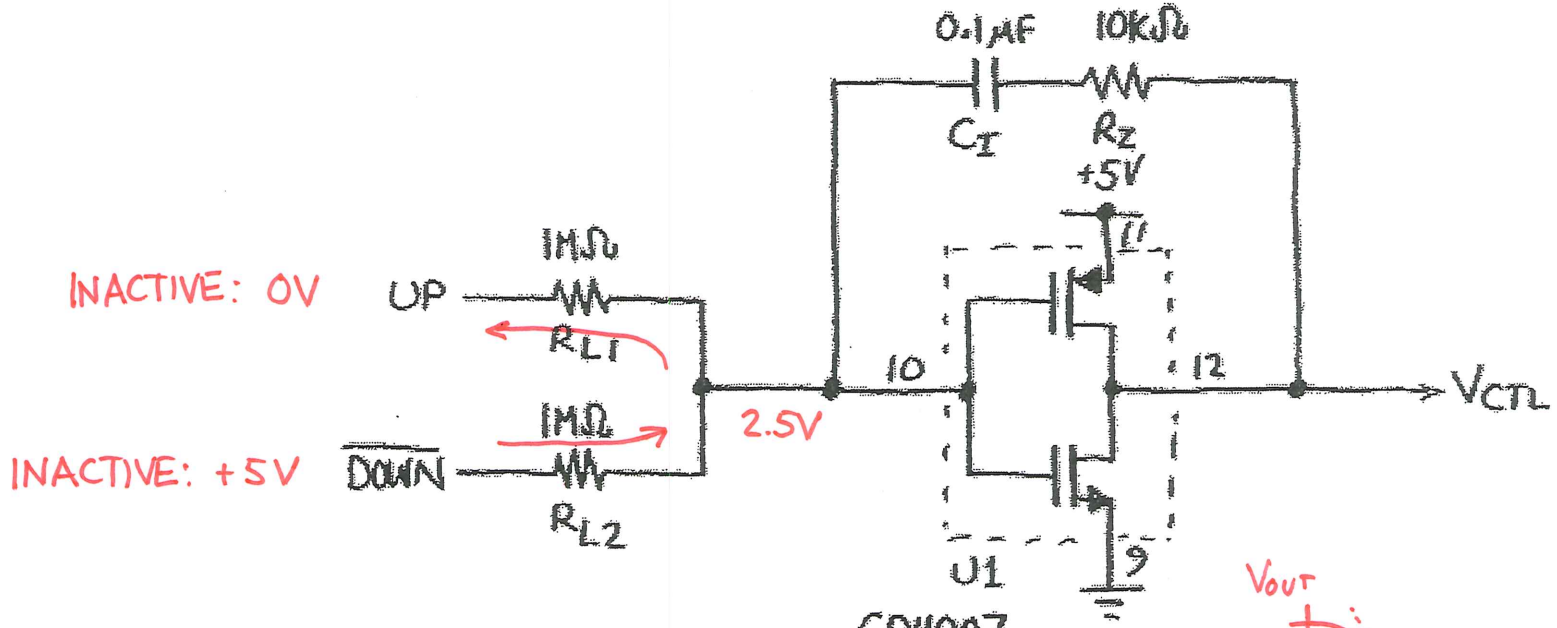


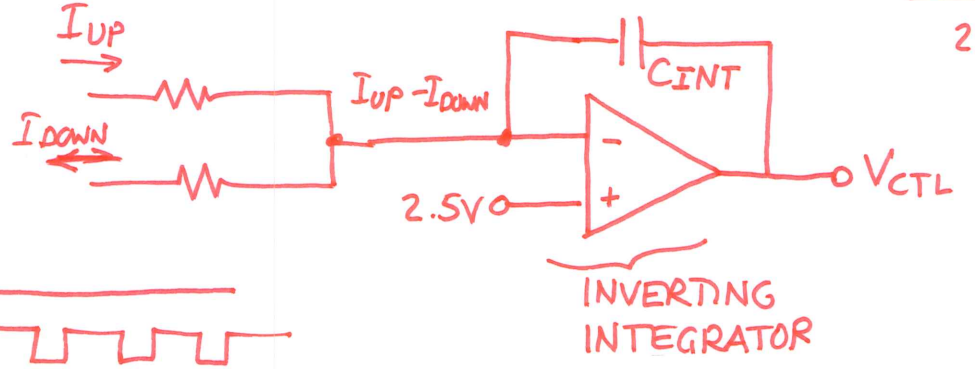


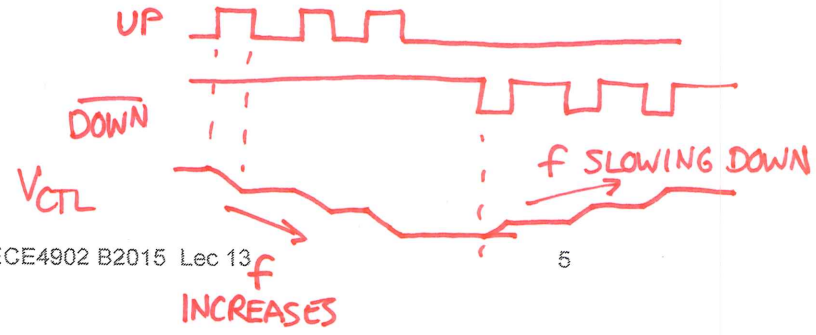
NEED TO SMOOTH OUT PULSES!

LOOP FILTER

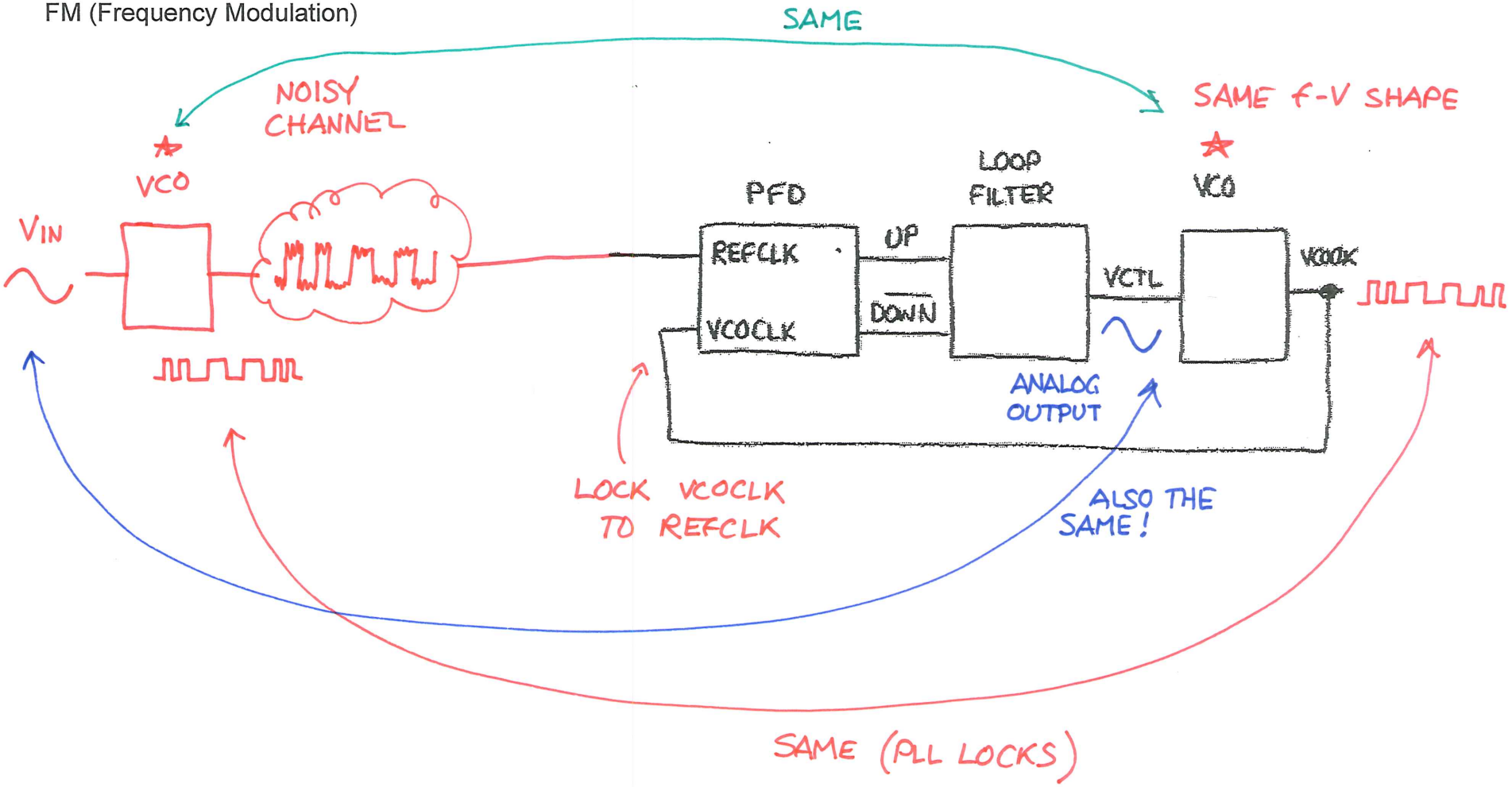
FINALLY: THE LOOP FILTER

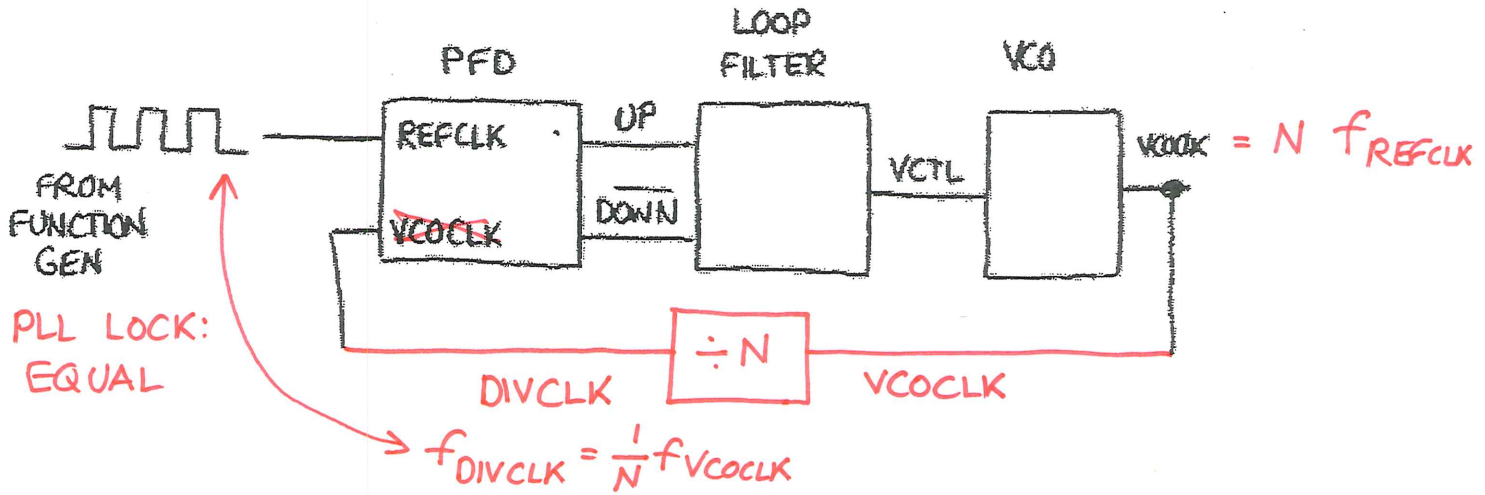


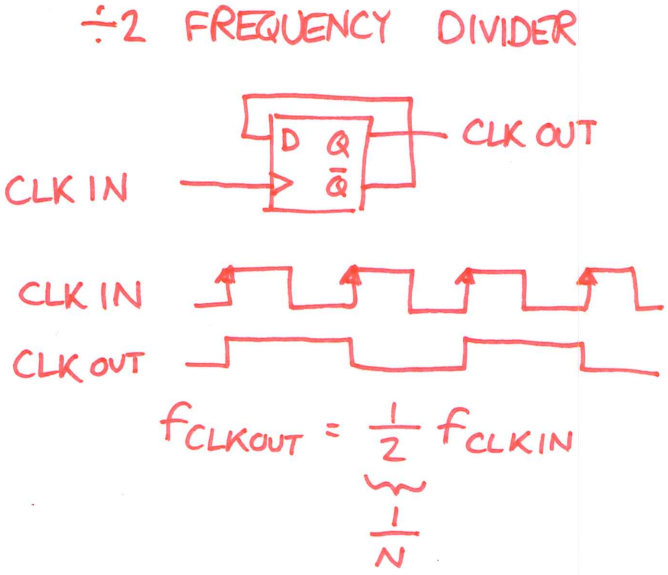


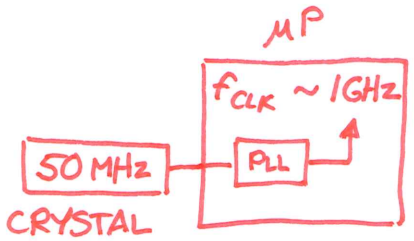


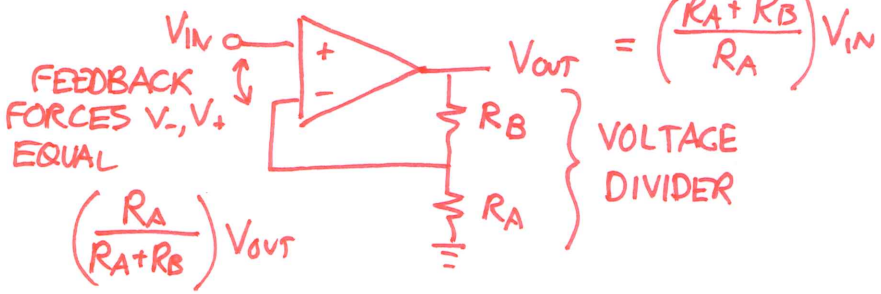
FM (Frequency Modulation)



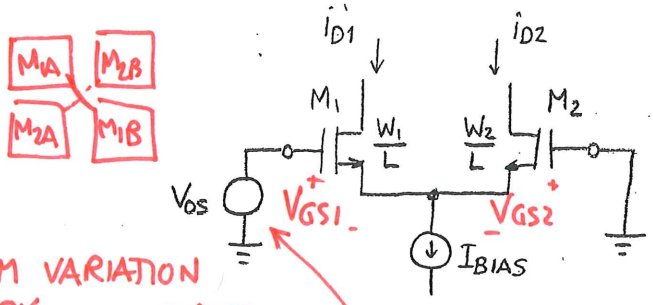

PFD
LOOP FILTER
VCO
REFCLK
VCOCLK
UP
DOWN
VCTL
VCOCLK
FROM FUNCTION GEN
PLL LOCK: EQUAL
÷N
DIVCLK
VCOCLK
$f_{DIVCLK} = \frac{1}{N} f_{VCOCLK}$
$= N\, f_{REFCLK}$

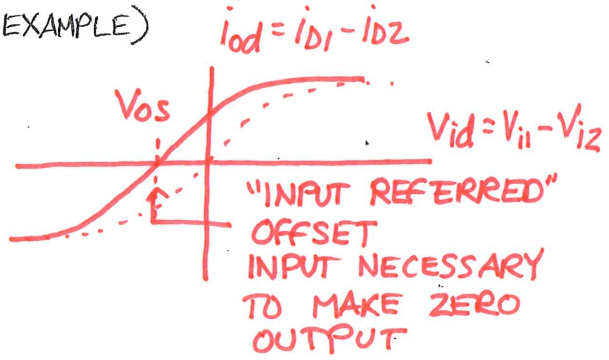

÷2 FREQUENCY DIVIDER
D
Q
$\bar{Q}$
CLK IN
CLK OUT
CLK IN
CLK OUT
$f_{CLKOUT} = \frac{1}{2} f_{CLKIN}$
$\frac{1}{N}$


μP
f_{CLK} ~ 1GHz
50 MHz
CRYSTAL
PLL


V_{IN}
FEEDBACK FORCES V_-, V_+ EQUAL
$V_{OUT} = \left(\frac{R_A + R_B}{R_A}\right) V_{IN}$
R_B
R_A
VOLTAGE DIVIDER
$\left(\frac{R_A}{R_A + R_B}\right) V_{OUT}$

DIFFERENTIAL PAIR OFFSET (W MISMATCH EXAMPLE)





RANDOM VARIATION IN MASK... μC_{ox} SAME

$W_2 > W_1 \Rightarrow i_{D2} > i_{D1}$ WITH ZERO INPUT V_{id}

NEED TO APPLY NONZERO V_{OS} TO "HELP" M1 $\Rightarrow i_{D1} = i_{D2}$

$$i_{D1} = \frac{\mu C_{ox}}{2}\frac{W_1}{L}\underbrace{(V_{GS} + V_{OS} - V_t)}_{V_{GS1}}{}^2 = i_{D2} = \frac{\mu C_{ox}}{2}\frac{W_2}{L}(V_{GS} - V_t)^2$$

} DEF OF INPUT REF'D V_{OS} IN SQUARE LAW

CANCEL COMMON TERMS; SOLVE FOR V_{OS}

$$W_1(V_{GS} + V_{OS} - V_t)^2 = W_2(V_{GS} - V_t)^2$$

⇓ REWRITE; MULTIPLY OUT

$$W_1\left[(V_{GS} - V_t) + V_{OS}\right]^2 = W_2(V_{GS} - V_t)^2$$

$$W_1(V_{GS} - V_t)^2 + 2W_1(V_{GS} - V_t)V_{OS} + \underbrace{V_{OS}^2}_{\text{SMALL}^2} = W_2(V_{GS} - V_t)^2$$

COMMON FACTOR

$$V_{OS} = \underbrace{\left(\frac{V_{GS} - V_t}{2}\right)}_{V_{eff}/2}\underbrace{\left[\frac{W_2}{W_1} - 1\right]}_{\to 0 \text{ IF } W_1 = W_2}$$ ✓

MISMATCH: $\Delta W = W_2 - W_1$ ERROR

AVG: $W = \frac{W_1 + W_2}{2}$ $W = W_1 = W_2$ IDEAL

EMPHASIZE MISMATCH

SUBSTITUTE $W_1 = W - \frac{\Delta W}{2}$ $W_2 = W + \frac{\Delta W}{2}$

SUB INTO V_{OS} EXPRESSION

$$V_{OS} = \frac{V_{eff}}{2}\left[\frac{W + \frac{\Delta W}{2}}{W - \frac{\Delta W}{2}} - 1\right] \Rightarrow \frac{V_{eff}}{2}\left[\frac{1 + \frac{1}{2}\frac{\Delta W}{W}}{1 - \frac{1}{2}\frac{\Delta W}{W}} - 1\right]$$

APPROX $\frac{1}{1-\varepsilon} \approx 1 + \varepsilon$

$$\Rightarrow \left[\left(1 + \frac{1}{2}\frac{\Delta W}{W}\right)\left(1 + \frac{1}{2}\frac{\Delta W}{W}\right) - 1\right]\frac{V_{eff}}{2}$$

SMALLER V_{eff} $(V_{GS} - V_{TH})$ OVERDRIVE

MULTIPLY OUT POLYNOMIAL

$$\left(1 + \frac{1}{2}\frac{\Delta W}{W} + \frac{1}{2}\frac{\Delta W}{W} + \left(\frac{\Delta W}{W}\right)^2 - 1\right)\frac{V_{eff}}{2} \Rightarrow \boxed{V_{OS} = \underbrace{\left(\frac{V_{eff}}{2}\right)}_{\text{VOLTAGE SCALE FACTOR}}\underbrace{\left(\frac{\Delta W}{W}\right)}_{\text{FRACTIONAL MISMATCH}}}$$

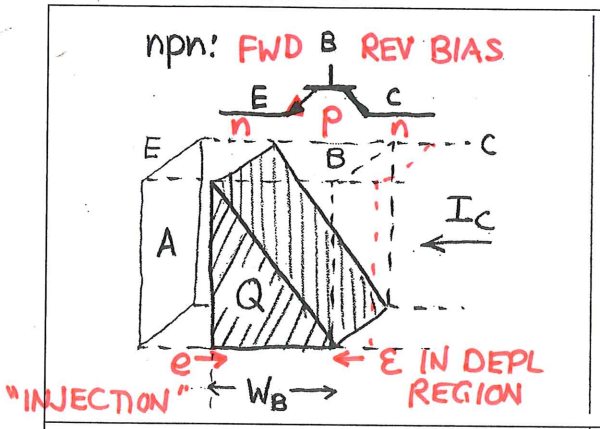
} FIXED DISTANCE (LITHOGRAPH ACCURACY)
} MAKE W BIGGER

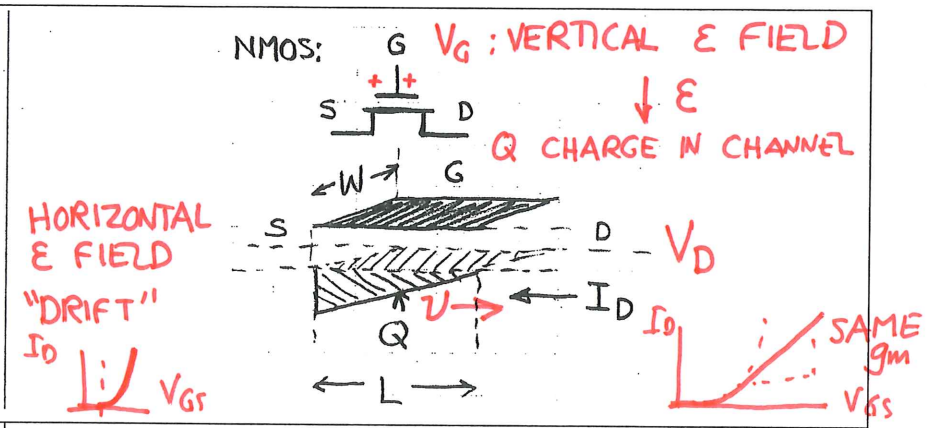
ORIGINAL DIFF PAIR

$V_{eff} = 0.25\,V$ $\frac{\Delta W}{W} = 1\%$ $\Rightarrow V_{OS} = 1.25\,mV$

ECE4902/4 MOS BJT Comparison

DIFFUSION





Current in collector terminal:	Current in drain terminal (active region):	
$I_C = \underbrace{\frac{qAD_n n_i^2}{2W_B N_A}}_{I_S} e^{(V_{BE}/V_T)}$ ($V_T = \frac{kT}{q}$)	Long channel ($L \gg 1\ \mu m$): MOBILITY $I_D = \frac{\bar{\mu} C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$	Short channel ($L \ll 1\ \mu m$): VELOCITY SATURATION $I_D = C_{OX} W v_{SAT}(V_{GS} - V_{TH})$ ○ LINEAR IN V_{GS} ○ NO L!
Representing current in form of I = Q/ΔT		
Charge in base: $Q = \frac{qAW_B n_i^2}{2N_A} e^{(V_{BE}/V_T)}$	Charge in channel: $Q = \frac{C_{OX} WL}{2}(V_{GS} - V_{TH})$	Charge in channel: $Q = C_{OX} WL(V_{GS} - V_{TH})$
Transit time through base: $\Delta T = \frac{W_B^2}{2\mu V_T}$	Transit time through channel: $\Delta T = \frac{L^2}{2\bar{\mu}(V_{GS} - V_{TH})}$	Transit time through channel: $\Delta T = \frac{L}{v_{SAT}}$ } MAX SPEED
Applied voltage:		
V_{BE}: Applied across base-emitter junction	V_{GS}: Applied from gate to source	
Geometry under designer control, subject to process (mask lithography) minimum:		
A: Base-emitter junction area	W: Width of channel under gate L: Length of channel under gate	
Process parameters:		
W_B: Width of base region (determined by diffusion of dopant atoms for base, emitter regions) N_A: Dopant density of p-type atoms in base	C_{OX}: Gate oxide capacitance per unit area (determined by thickness, dielectric constant of gate oxide) V_{TH}: Threshold voltage (determined by lots of things; see Razavi ch. 16)	
Physical parameters:		
μ: **Bulk** mobility of carriers in base D_n: Diffusion constant of electrons in base n_i: Intrinsic carrier concentration (strongly temperature dependent q: Electron charge V_T: thermal voltage = kT/q ~ 26mV @ T=300K	$\bar{\mu}$: **Surface** mobility of carriers in channel	v_{SAT}: Saturation velocity (maximum due to high field; ≈ 1E+7 cm/s.

ECE4902 MOS BJT Comparison

Notes:

Speed

W_B, L are critical dimensions for improving speed performance

Note exponent of 2 in ΔT equation indicates that improvement goes as factor squared; meaning there are two reasons speed improves:

1) Shorter distance for carrier to travel
2) More "push" (steeper diffusion gradient for BJT, higher E field for MOSFET in long channel limit)

Factors in MOS - BJT speed performance:

1) Bulk mobility (BJT) always better than surface mobility (MOSFET)
2) Reducing critical dimension involves different process considerations
3) Trying to increase MOSFET speed by increasing V_{GS}-V_{TH} has two problems:
   - reduces transconductance efficiency
   - carrier velocity doesn't increase as much as expected due to velocity saturation (Razavi ch. 16)

Small signal transconductance g_m:	
$g_m = \frac{I_C}{V_T}$ } MORE g_m PER I_{BIAS} 26mV	$g_m = \frac{I_D}{(V_{GS} - V_{TH})/2}$ 100 mV SUBTHRESHOLD

Why BJT transconductance will always be better for roughly similar bias currents:

Thermal voltage V_T is less than (V_{GS}-V_t); trying to reduce V_{GS}-V_t below ~ 150mV causes MOSFET to enter subthreshold (weak inversion) region of operation

Advantages of MOS:

Near ∞ input resistance looking into gate vs. base current for BJT (better buffer on input side)
Better analog switch; truly ohmic at origin of V_{DS}-I_D plot (sample & hold)
Compatible with digital CMOS (process cost advantage)
Comes out of non-active operating region more quickly (BJT slow out of saturation)
More robust current sources (gentler "crash" than BJT into saturation)

Advantages of BJT

More speed, transconductance per amount of bias current
Higher intrinsic gain for actively loaded stage (better Early voltage)
Lower output resistance at emitter vs. source of MOSFET (better buffer on output side)
"Closer" to fundamental physics (e.g. bandgap voltage reference)
Follows exponential model over 5 - 8 orders of magnitude (analog computation; multipliers)
Higher output resistance current sources

FINAL EXAM:

OP-AMP:

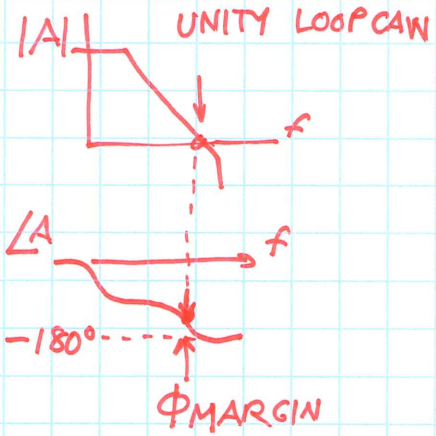
DC ANALYSIS: I_D, V_{GS} OPERATING POINT ; OUTPUT SWING LIMIT (TRIODE CRASH)

+, − INPUTS

DOMINANT POLE MODEL: $f_T = \frac{g_m}{2\pi C_{COMP}}$ $SR = \frac{I_{BIAS}}{C_{COMP}}$

STABILITY ANALYSIS (2 POLE MODEL)

$|A|$, $\angle A$ PHASE MARGIN



DIFF PAIR DESIGN FOR DC OUTPUT
GAIN
SIGNAL SWING