Studio 1 Review

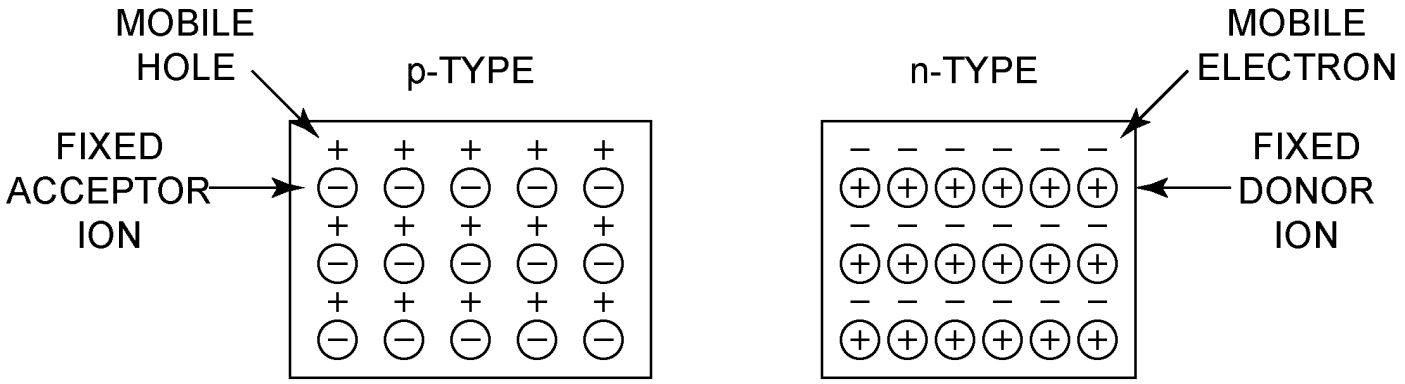
- **P-N Junction Diode**
  - **Reverse bias diode junction capacitance**
- **MOSFET**
  - **Physical construction; Circuit symbols**
- **Lab Exercise**
  - **PN junction capacitance**
  - **MOSFET Gate capacitance**
- **Text Readings:**
  - **Razavi**
    - **Sec. 2.1-2 pp. 9-23**
  - **Johns & Martin**
    - **Sec. 1.1 pp. 1-12**
    - **Sec. 1.2 pp. 16-20; Sec 2.1 pp. 82-94**

P-N Junction Diode

- **Junction between p-type, n-type materials**
- **Assume structure is simple enough that we can consider only one spatial dimension**
- **Model: only consider "extra" charges**
- **Mobile charges contributed by dopants: each mobile charge was contributed by a fixed charge of opposite sign**

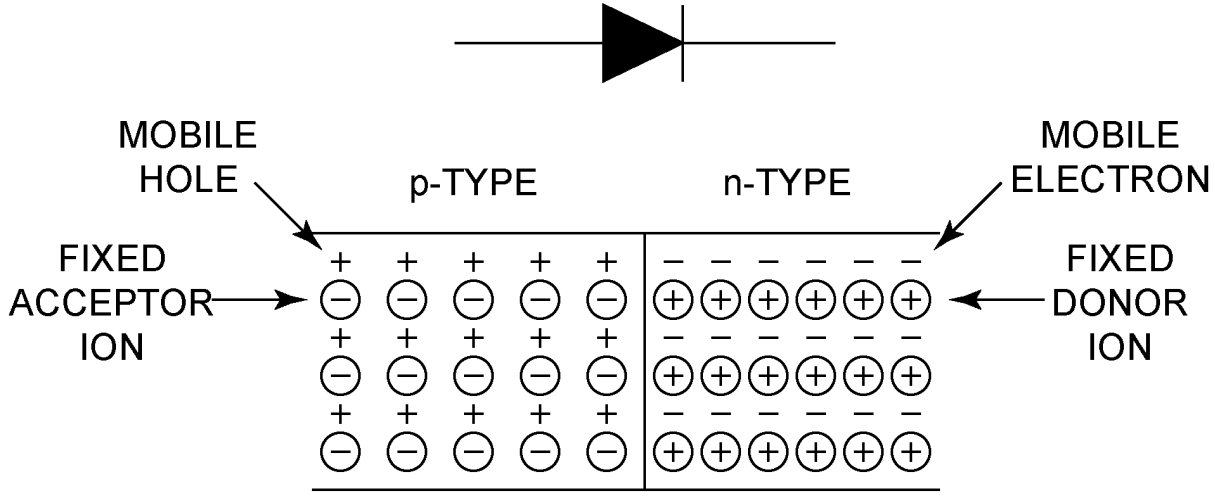
P-N Junction Diode

- **Thought experiment: take isolated p-type, n-type and bring together**



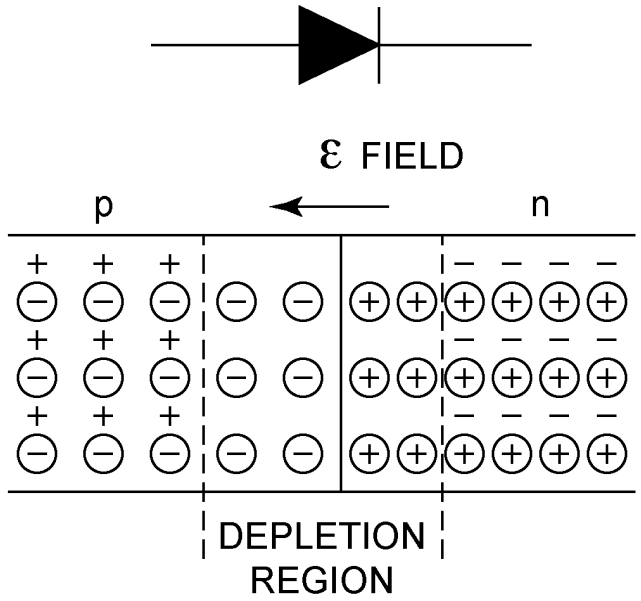
$V_A = 0$ (t=0)

- **No electric field; Thermal diffusion**



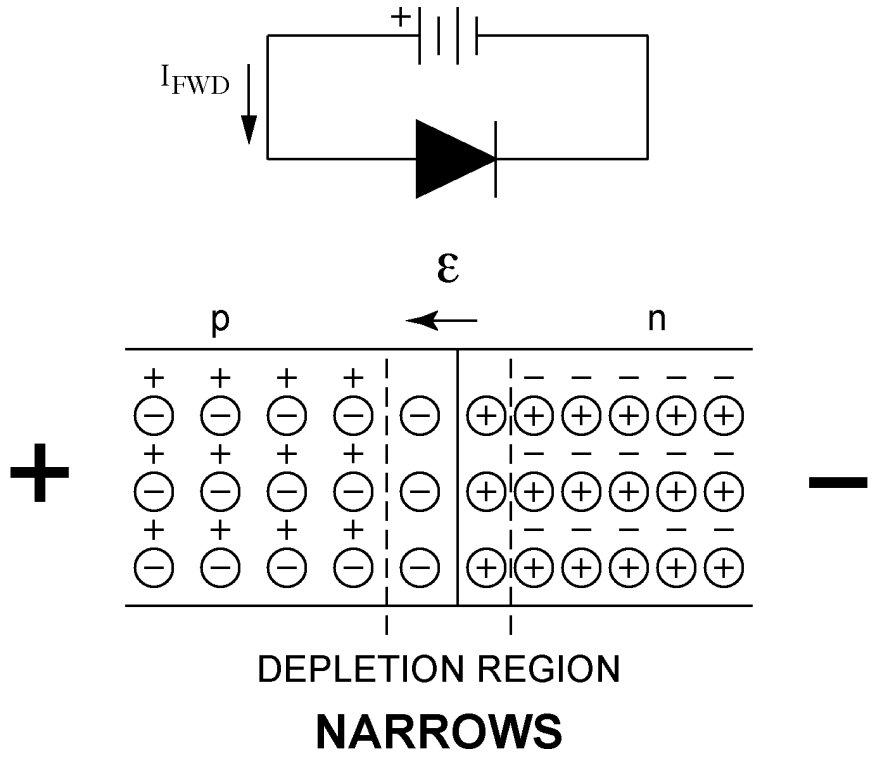
$V_A = 0$ (equilibrium t > 0)

- **Internal electric field balances diffusion**



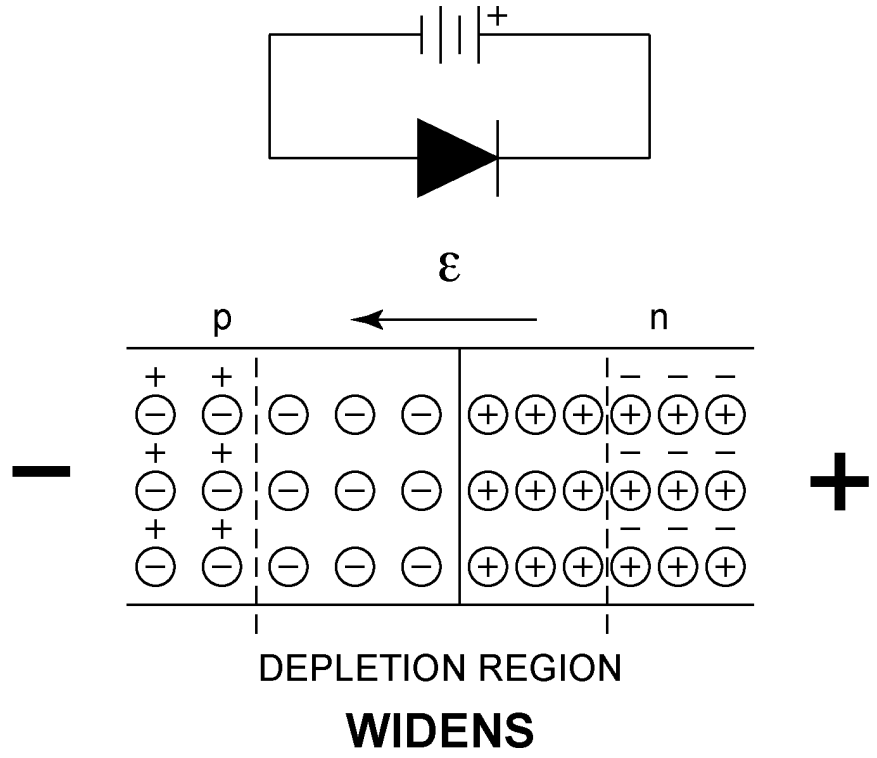
V_A positive (forward bias)

- **Applied V_A "overpowers" internal E field**



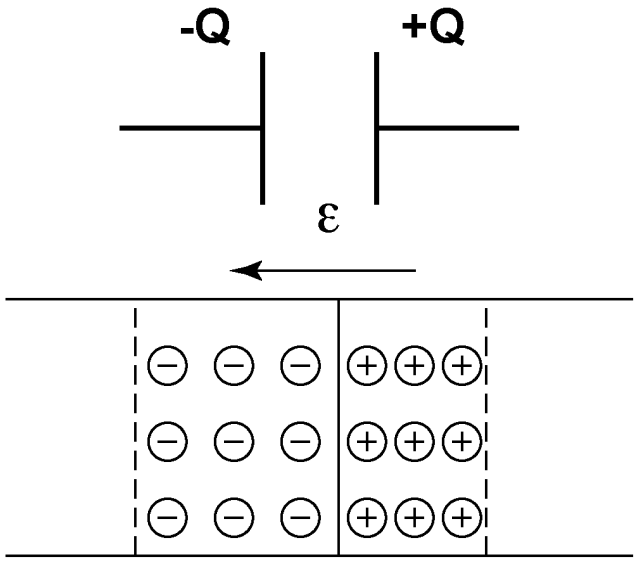
V_A negative (reverse bias)

- **Applied V_A "reinforces" internal E field**
- **Field "pulls" mobile charges further apart**



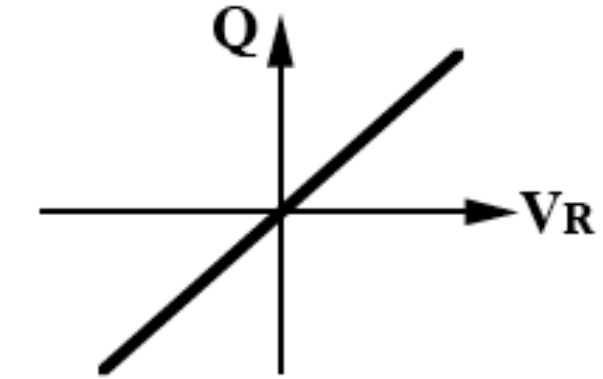
Junction Capacitance

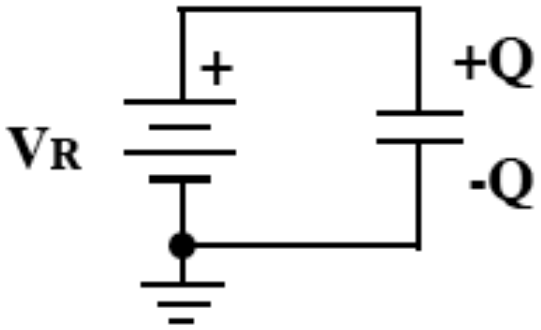
- **Equal and opposite charges, physically separated, changes with voltage: Capacitance!**



Junction Capacitance

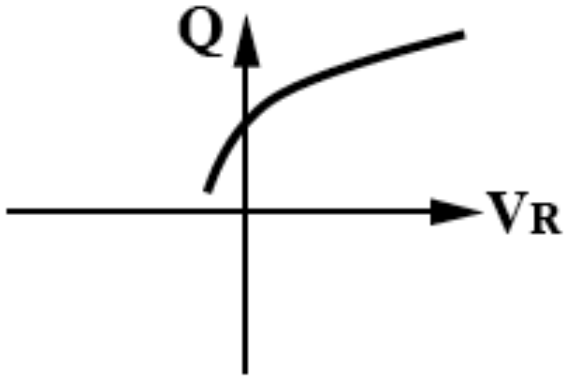
$$C = dQ/dV$$

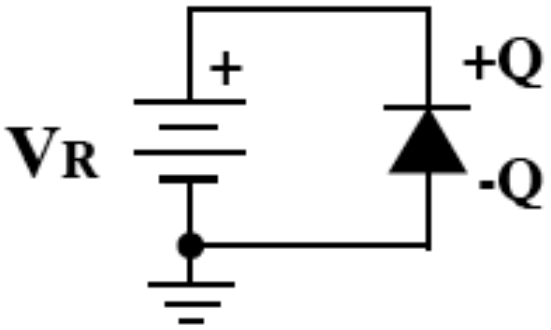




Same slope for any V

Linear capacitance





Slope depends on V

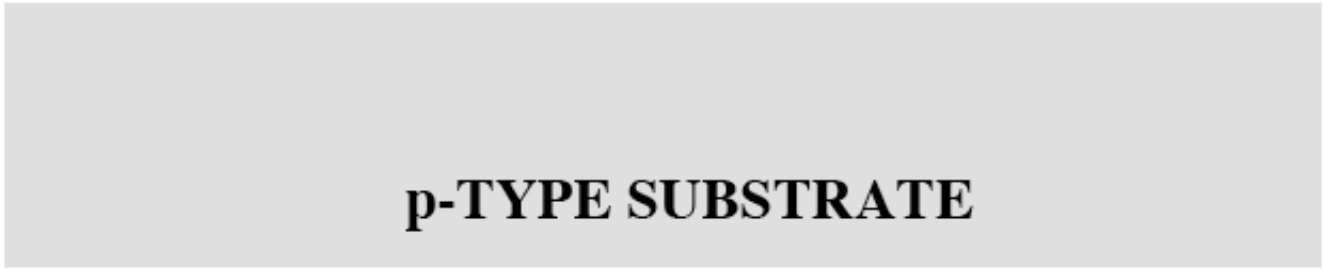
<u>Nonlinear capacitance</u>

Semiconductor Physics Review Summary

- **Conduction in semiconductor:**
  e- and "holes"(absence of electrons)
- **N region has mostly mobile electrons;**
  P region has mostly mobile "holes"
- **PN junction has a depletion region**
  (no mobile carriers)
- **Size of the depletion region depends on the applied voltage and the P, N doping**
- **Reverse biased PN junction acts like a nonlinear capacitor**

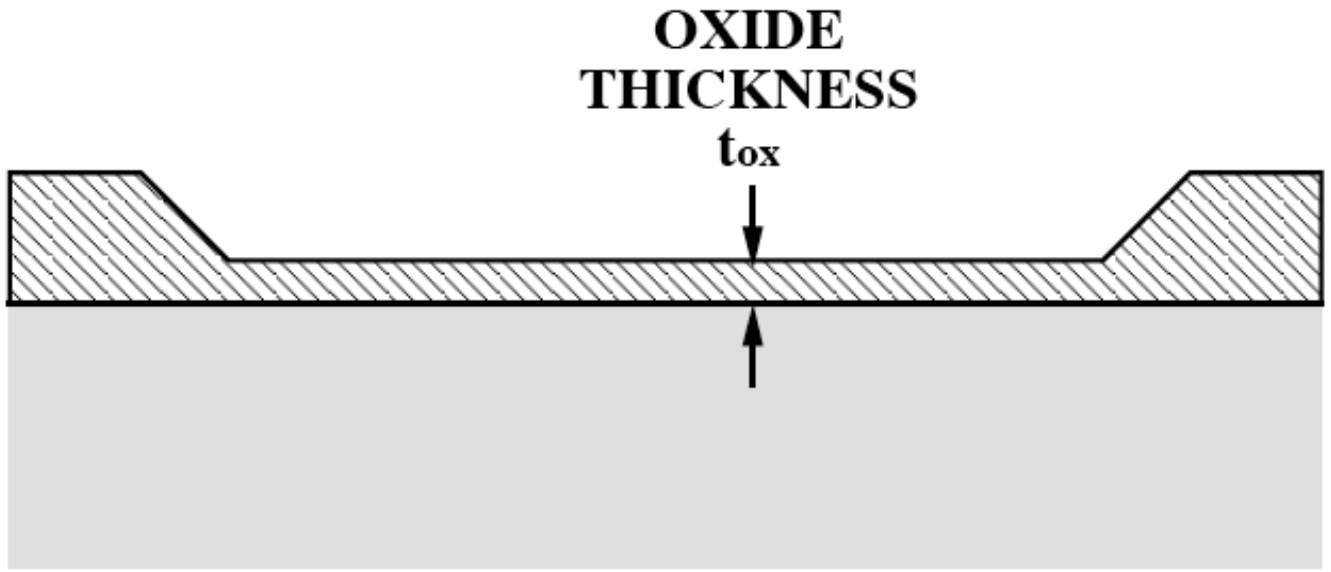
n-channel MOSFET Simplified Construction

- **Start: Silicon Substrate lightly doped p-type**
- **Cross-sectional view**



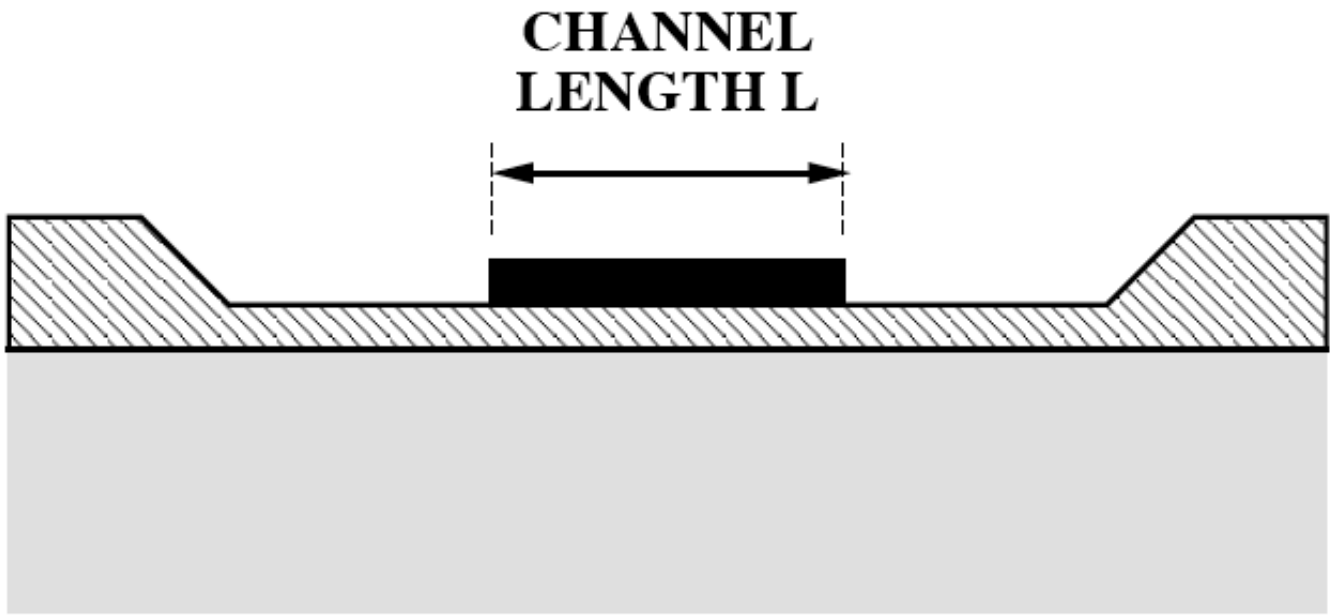
Deposit Oxide

- **Thin in "active area" of MOSFET (defines W)**
- **t_{ox} oxide thickness**
- **Thick elsewhere (insulate from substrate)**



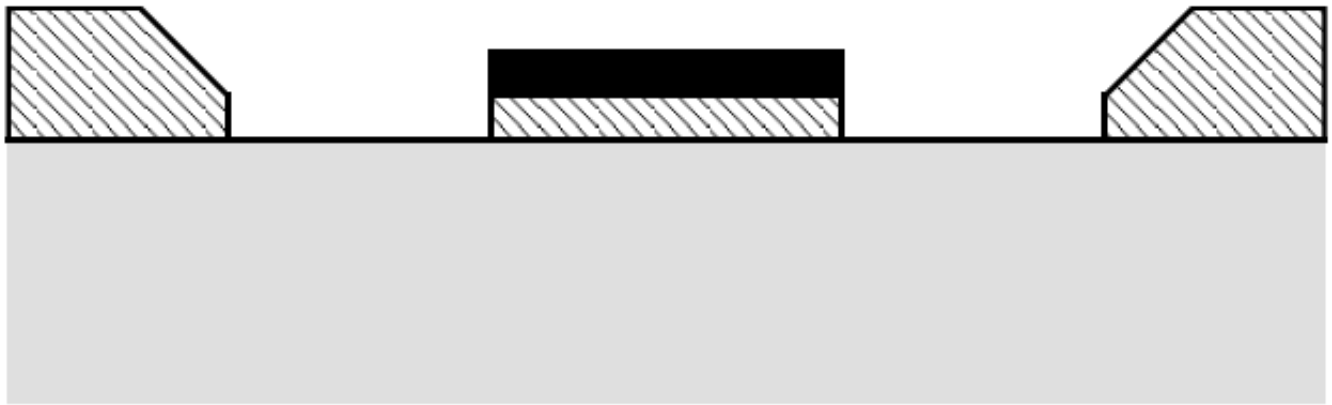
Deposit Gate polysilicon

- **Defines length L of channel**



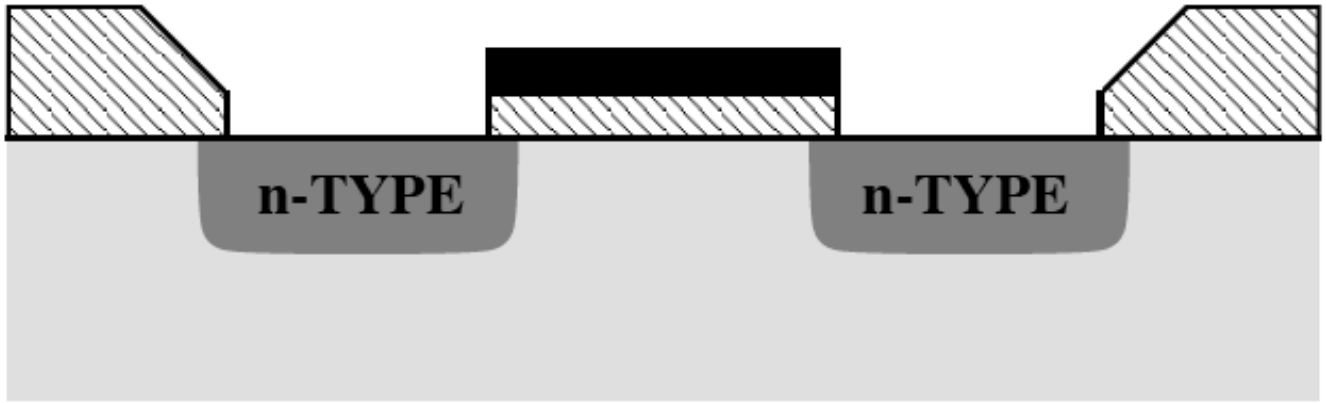
Open Source, Drain areas

- **Etch away areas of thin oxide not covered by gate ("self-aligned")**



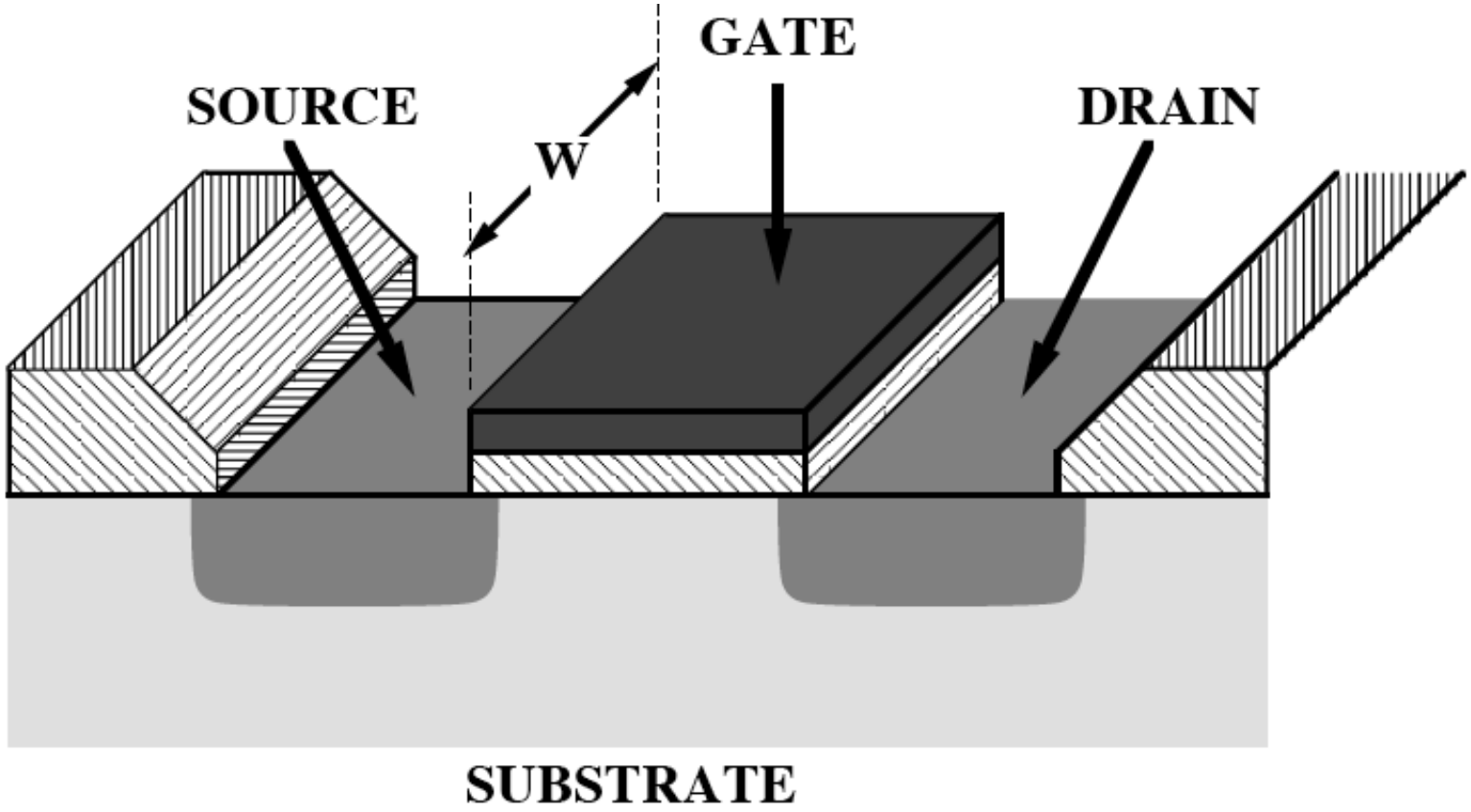
Implant Source, Drain regions

- **Dope n-type**



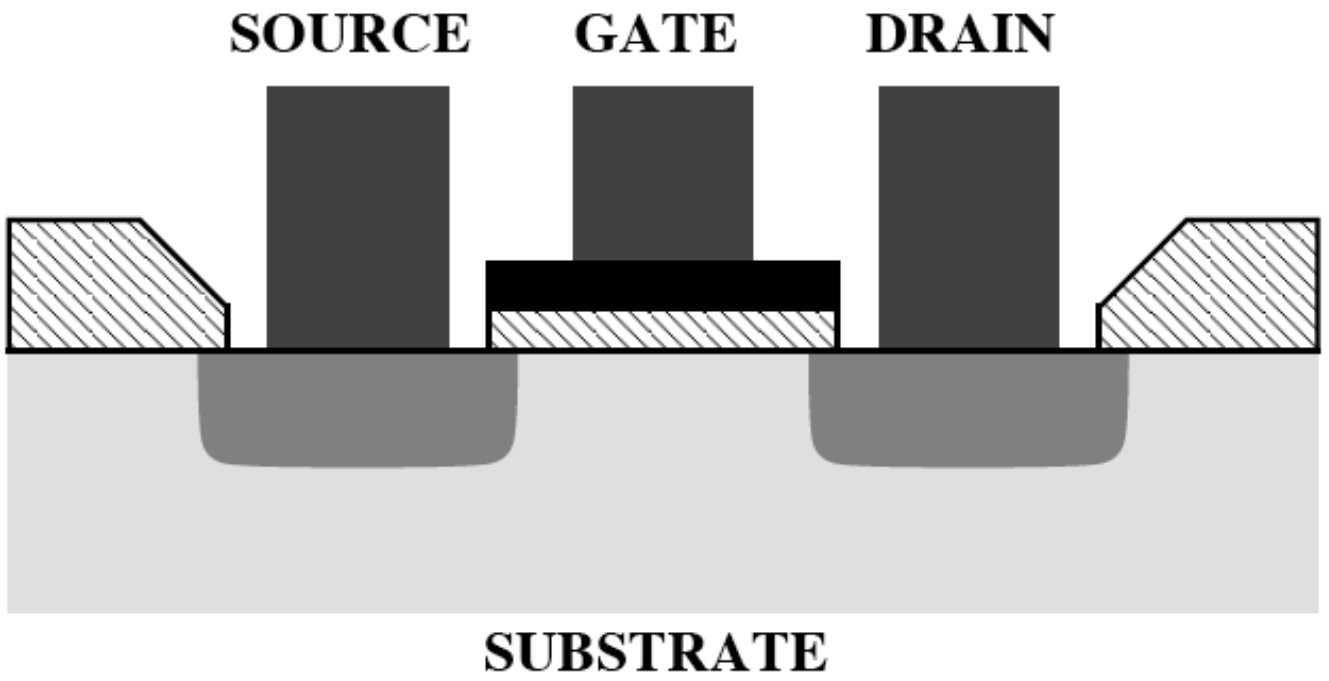
3-D View

- **Channel width W**



Contact G, S, D

- **Aluminum metallization**

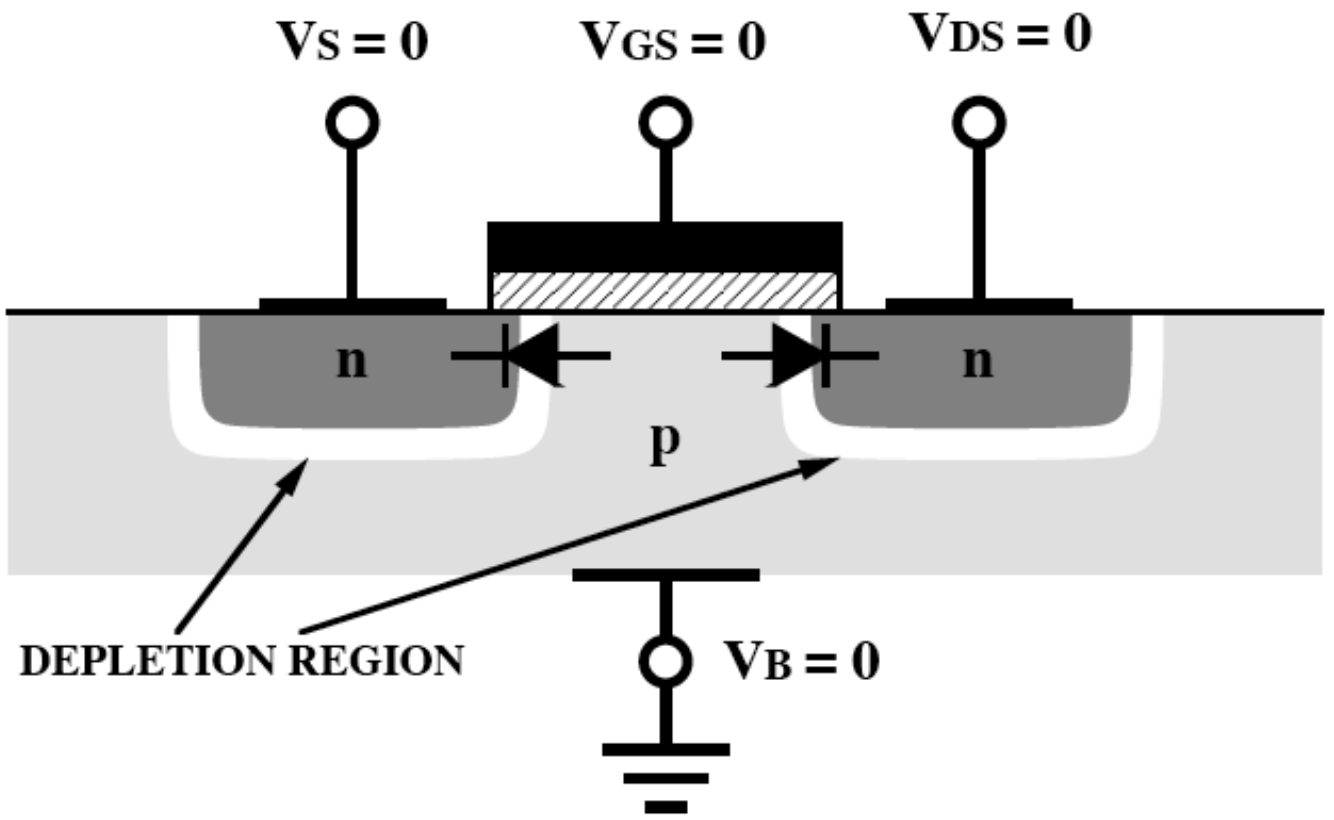


Handwaving operation (n-channel)

- $V_{GS} = 0$ S-D channel "off"
- $V_{GS} > V_{TH}$ (threshold voltage) S-D channel "on"

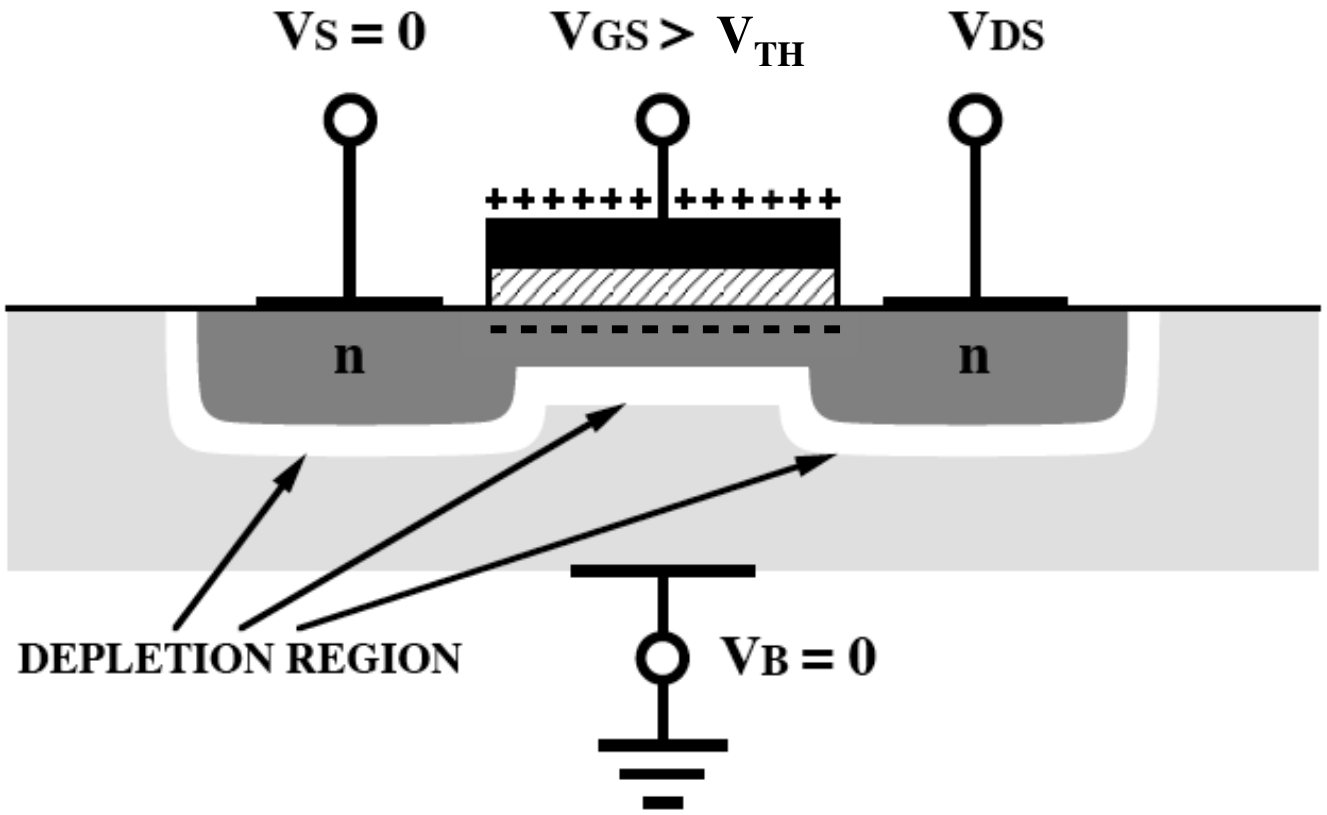
$V_{GS} = 0$ S-D channel "off"

- **Back-to-back reverse bias diodes**



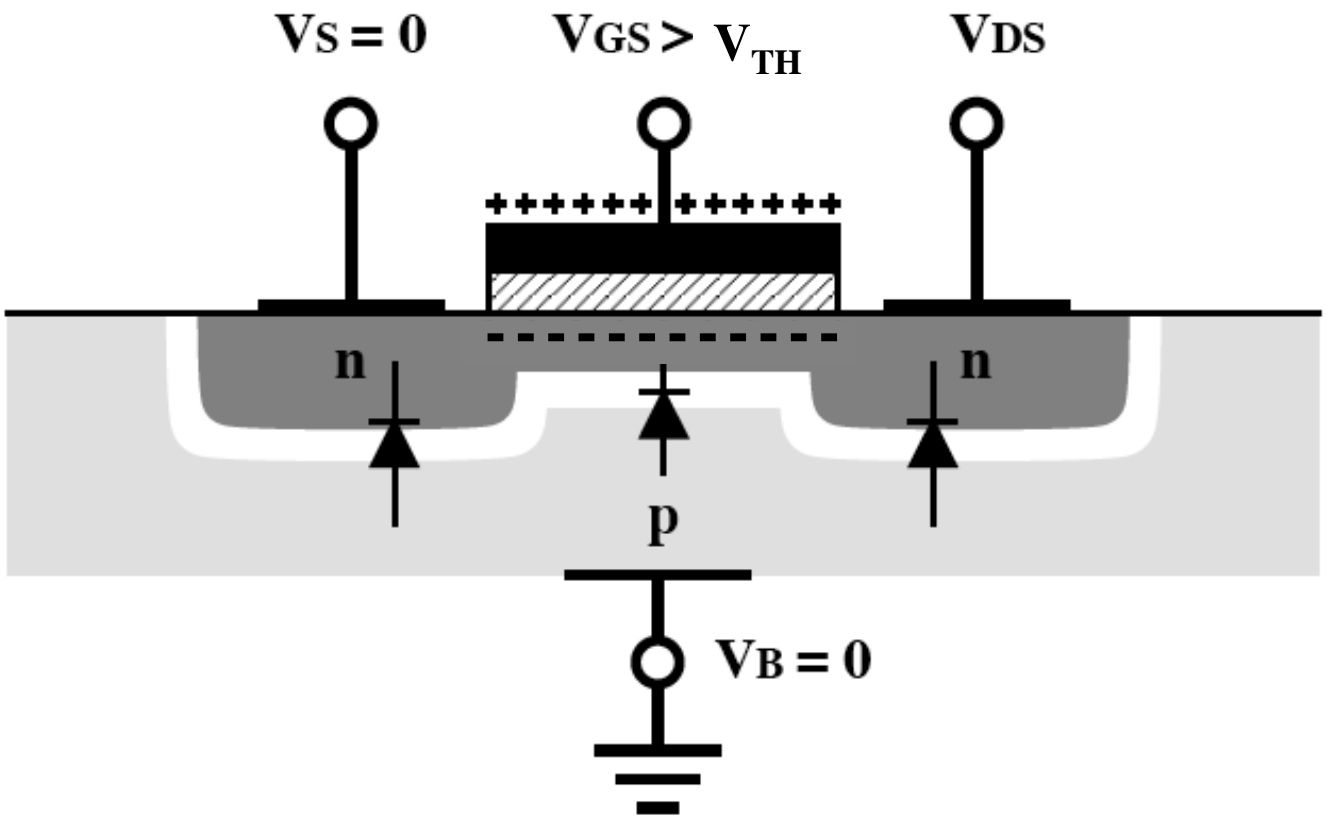
$V_{GS} > V_{TH}$ (threshold voltage) S-D channel "on"

- **If we apply V_{DS}:**
  conducting channel S-D, current can flow



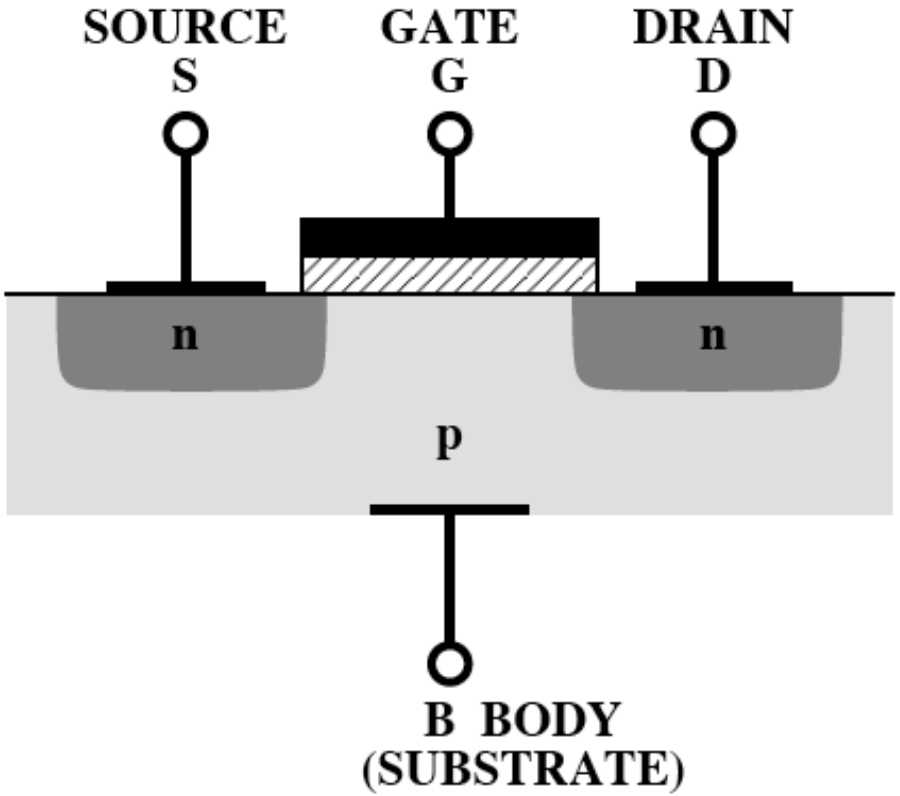
Substrate junction

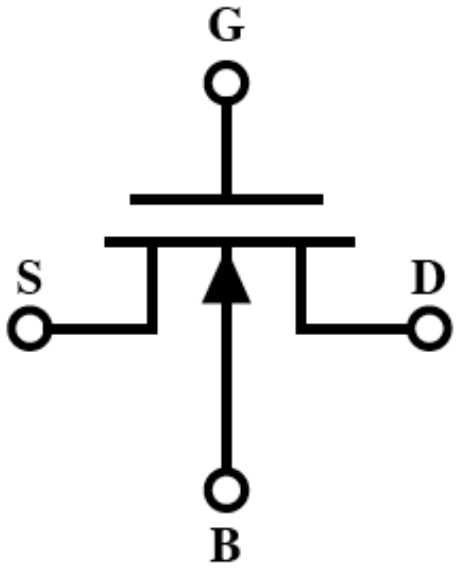
- **Must always be reverse biased!**



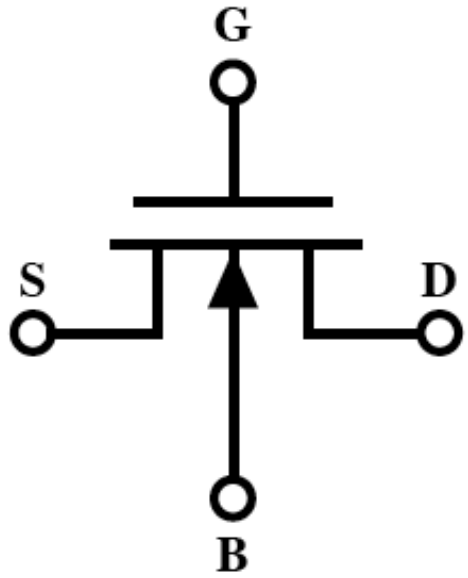
Circuit symbols: n-channel

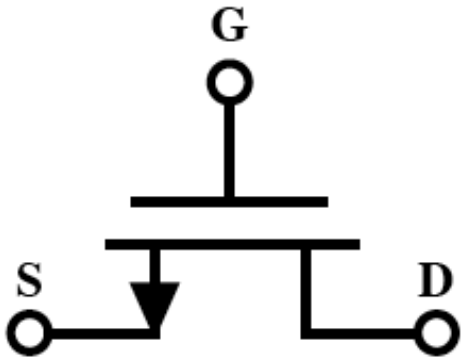
- **4-terminal symbol: show substrate explicitly**





Circuit symbols: n-channel
Note different meaning of arrow!

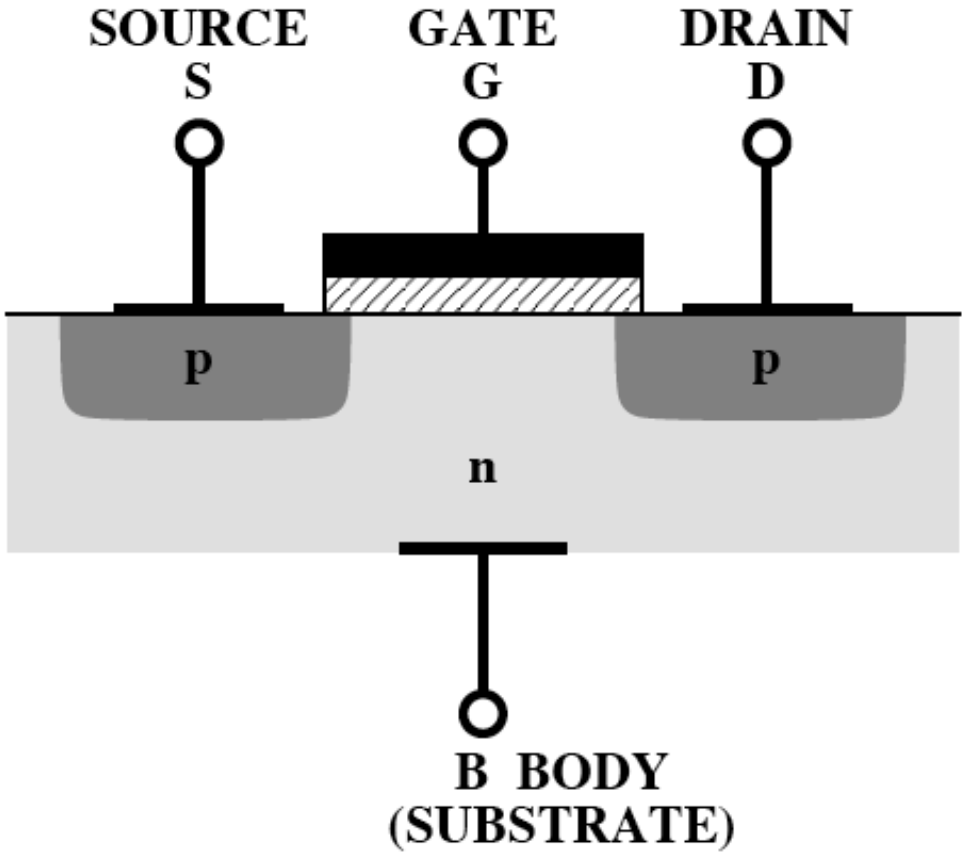


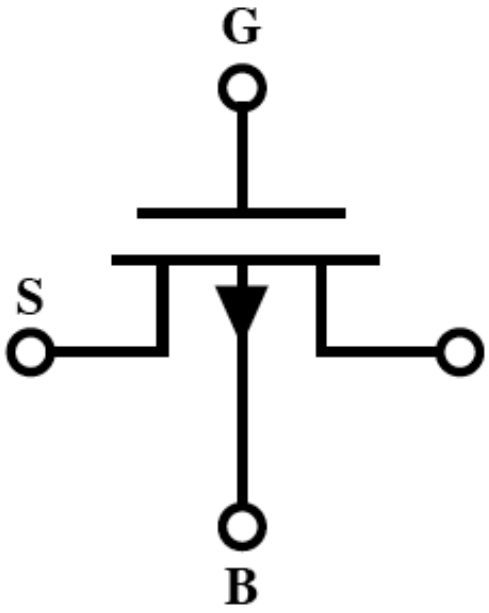


- **4 terminal**
  Arrow shows direction of substrate-channel pn junction
- **3 terminal**
  Arrow shows direction of positive current flow at source terminal

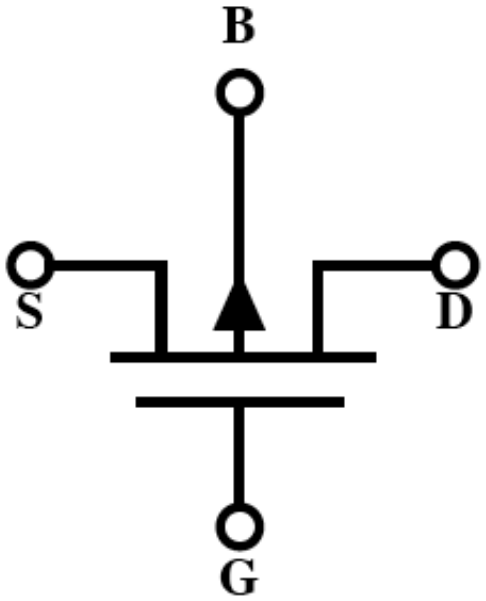
Circuit symbols: p-channel

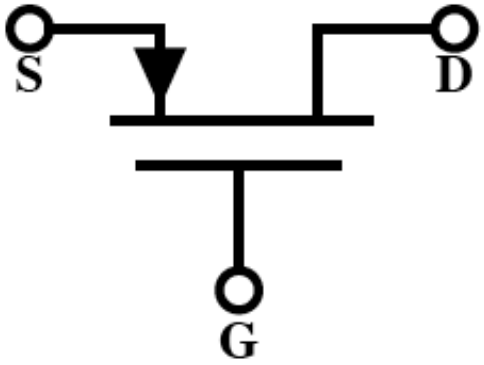
- **4-terminal symbol: show substrate explicitly**





Circuit symbols: p-channel
Note different meaning of arrow!





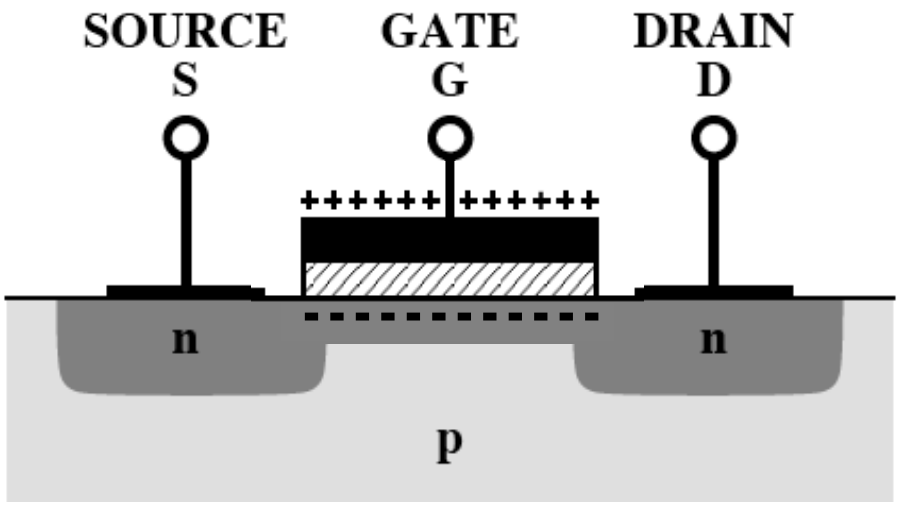
- **4 terminal**
  Arrow shows direction of substrate-channel pn junction
- **3 terminal**
  Arrow shows direction of positive current flow at source terminal

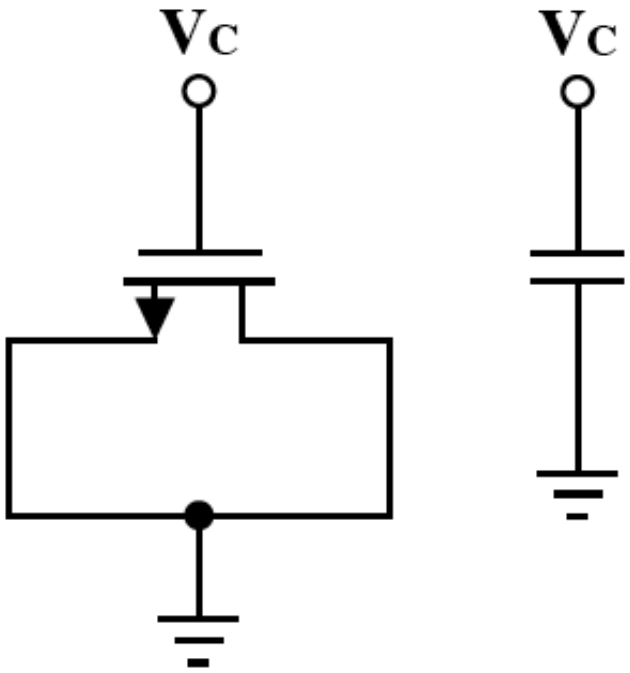
MOSFET functions

- **Analog switch**
- **Digital switch**
- **Amplifier**
- **Buffer**
- **Current source**
- **Resistor**
- **Capacitor**

Capacitor

- **MOS Gate capacitance**





Summary

- **MOSFET construction**
- **Gate voltage controls Drain-Source behavior**
- **Gate: "Looks like" capacitance**
- **Drain-Source can be conductive channel**
- **Threshold voltage V_{TH}**
- **Substrate junctions must always be reverse biased**
- **Lab: Oxide thickness t_{ox}**

Gate Capacitance

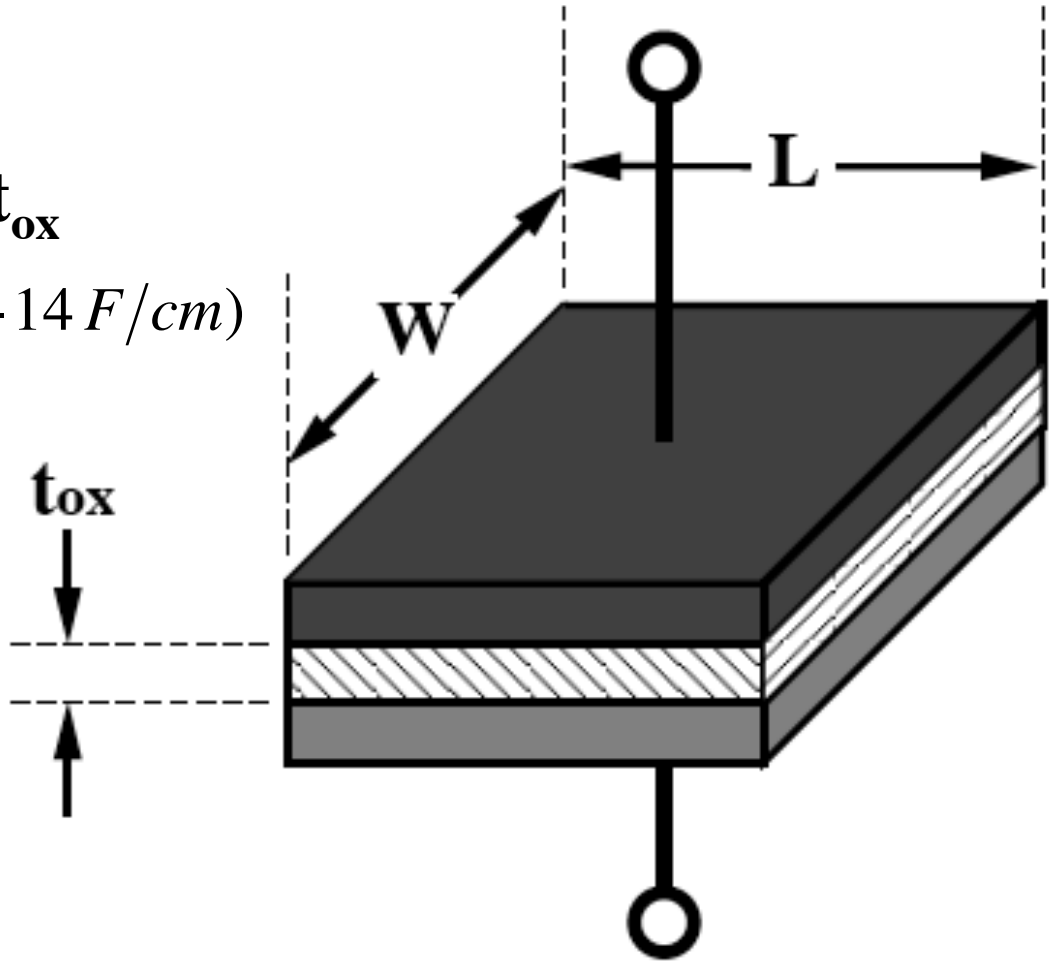
- **Parallel plate capacitance**

$$C = \frac{\varepsilon A}{d}$$

- **MOSFET: A=WL**
- **d= oxide thickness t_{ox}**

$$\varepsilon = K_{ox}\varepsilon_0 = (3.9)(8.85E-14\,F/cm)$$

$$C_{gs} = \frac{K_{ox}\varepsilon_0 WL}{t_{ox}}$$



Lab exercise

- **Determine t_{ox} for CD4007 MOSFET array**
- **Known:**
  n: W=350um, L=10um
  p: W=900um, L=10um
- **Use risetime method to measure capacitance of all gates in parallel (3 N-ch, 3 P-ch on chip)**
- **$C_{(gs)TOTAL} = 3\ C_{gs(n)} + 3\ C_{gs(p)}$**
- **Repeat without MOSFET chip to get fixture capacitance**
- **Record for use in models later!**