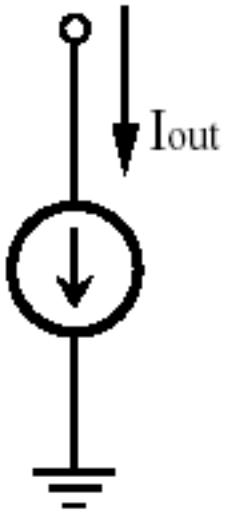
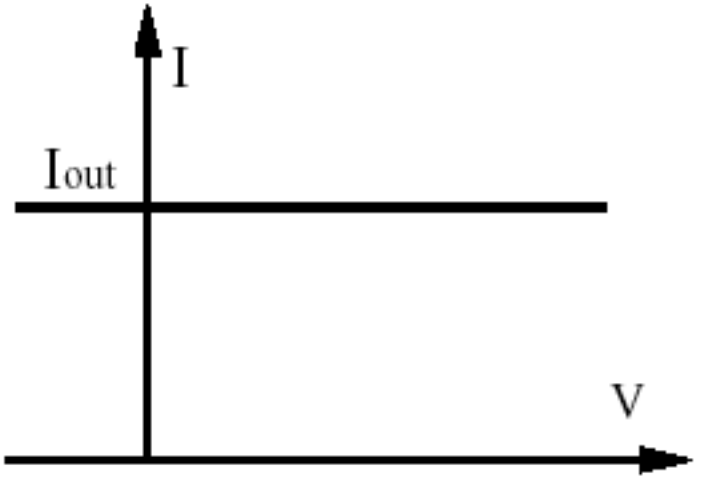
# Lab 5 Review Slides

- **Current Source**
- **Active Load**
- **Bandwidth of Common Source Amplifier**

# Current source

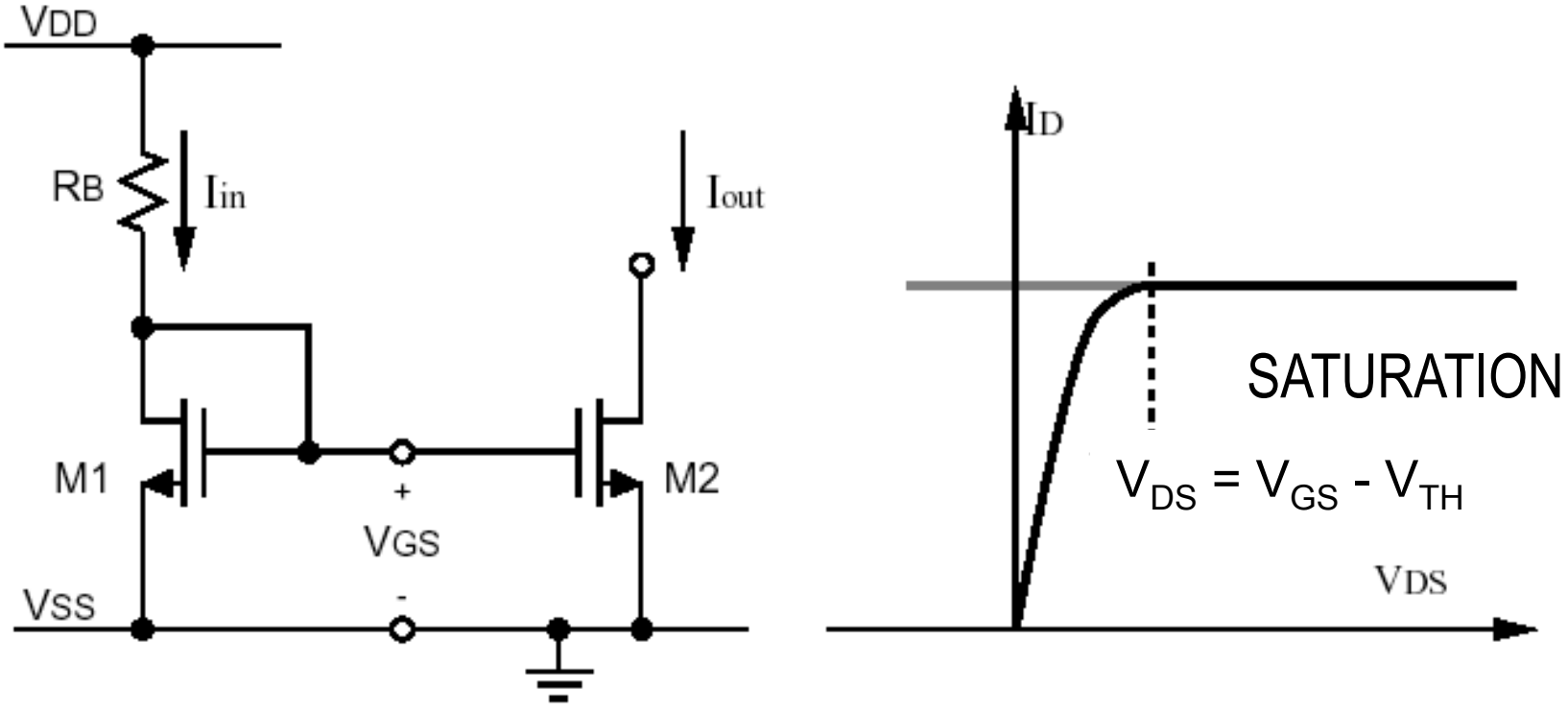
- **Ideal goal**
- **Small signal model: Open circuit "$R_D=\infty$"**



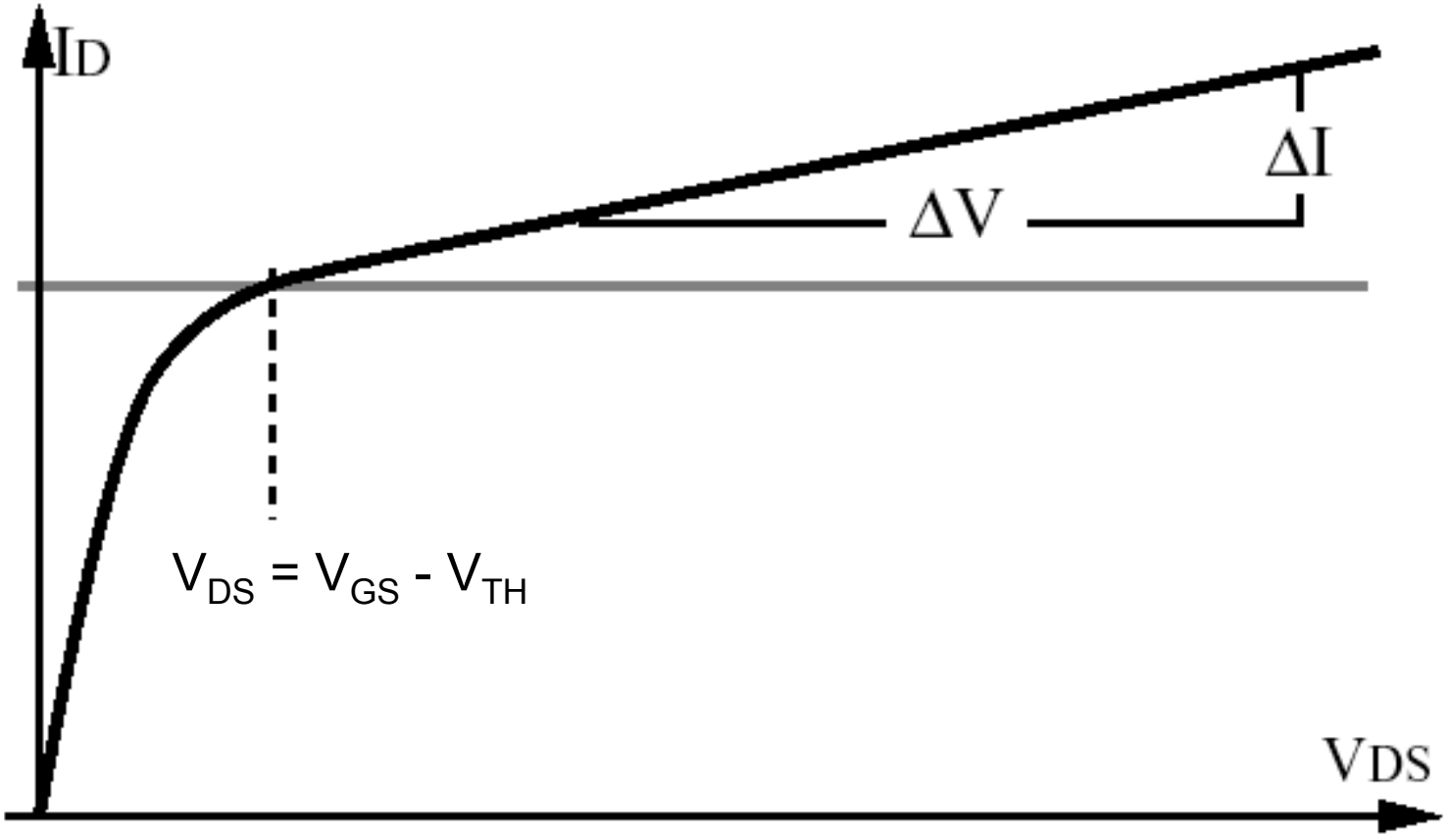
# Realizing current source: MOSFET

- **Large signal nonideality: "Compliance range"**
- **Looks like current source only for $V_{DS}>V_{GS}-V_{TH}$**



# MOSFET $I_D$-$V_{DS}$ characteristic for fixed $V_{GS}$

- **Small-signal nonideality: slope in active region**

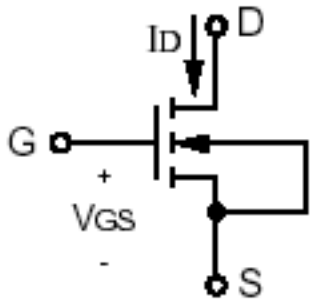


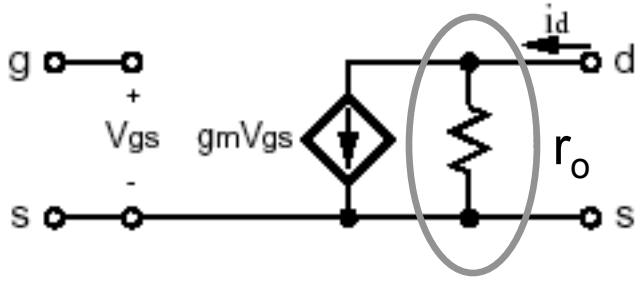
# Modify small-signal model: Finite $r_{ds}$ current source

- **Slope = ΔI/ΔV**

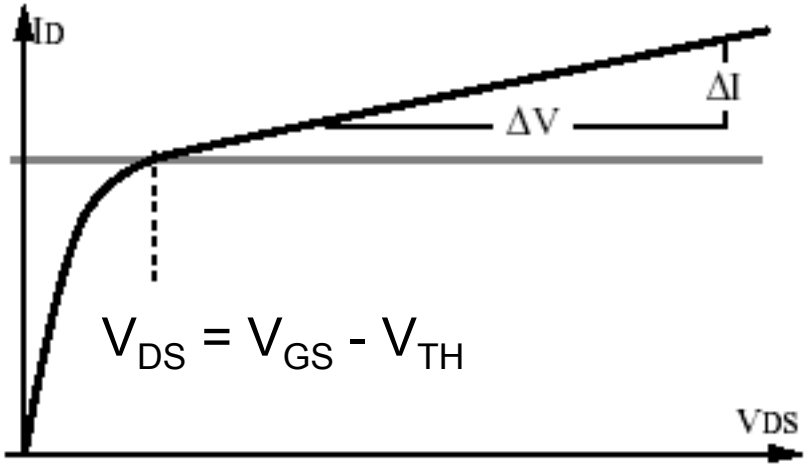
$$r_o = \frac{\Delta V}{\Delta I}$$

$$SLOPE = \frac{\Delta I}{\Delta V} = \frac{1}{r_o}$$

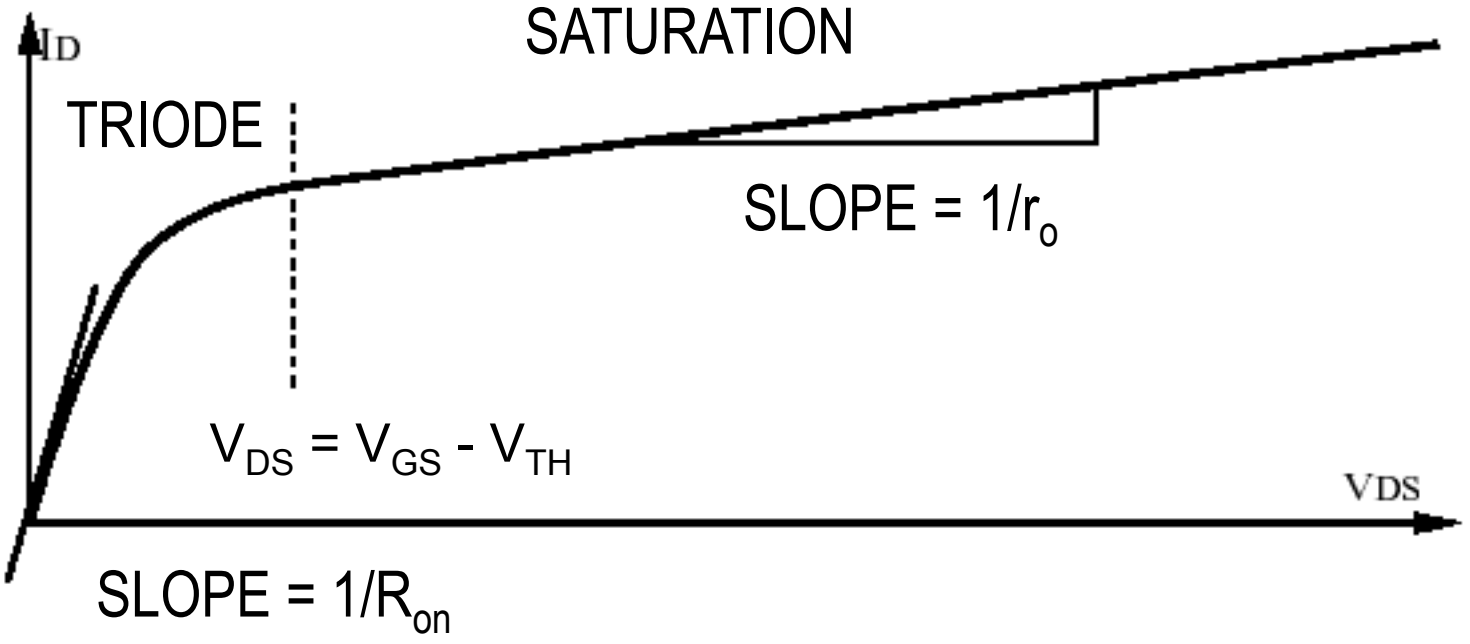



- **Ideal:**
  **zero slope**
  **⇒ $r_o = \infty$**



# Caution: $R_{on}$ vs. $r_o$ confusion!



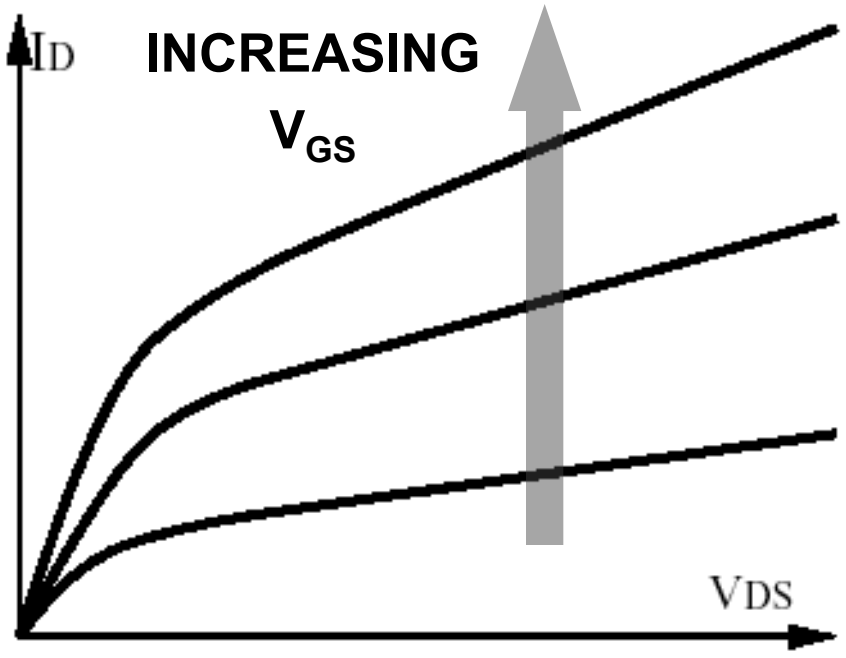

**$R_{on}$**

- **Triode region**
- **Large signal**
- **True resistance (V-I through origin)**

**$r_o$**

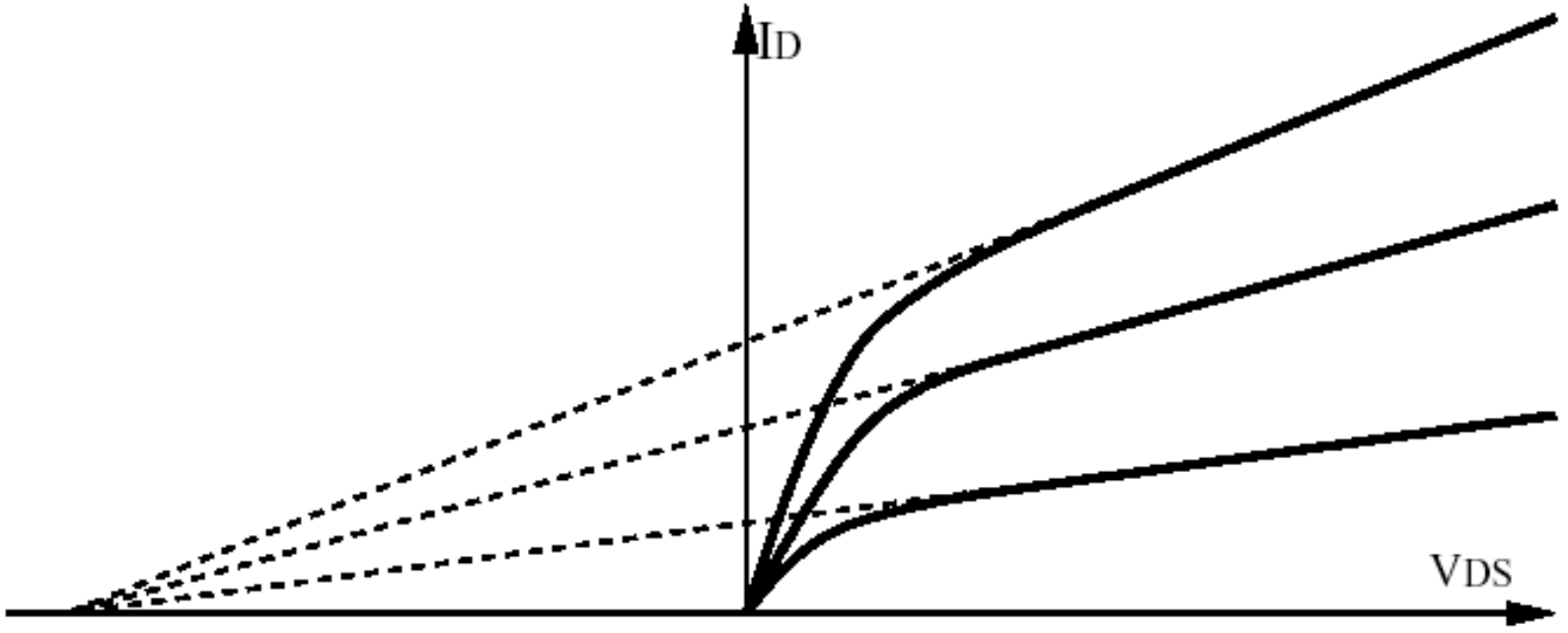
- **Saturation region**
- **Small signal**
- **Models nonideality of current source**

# $I_D$- $V_{DS}$ Characteristic for Different $V_{GS}$



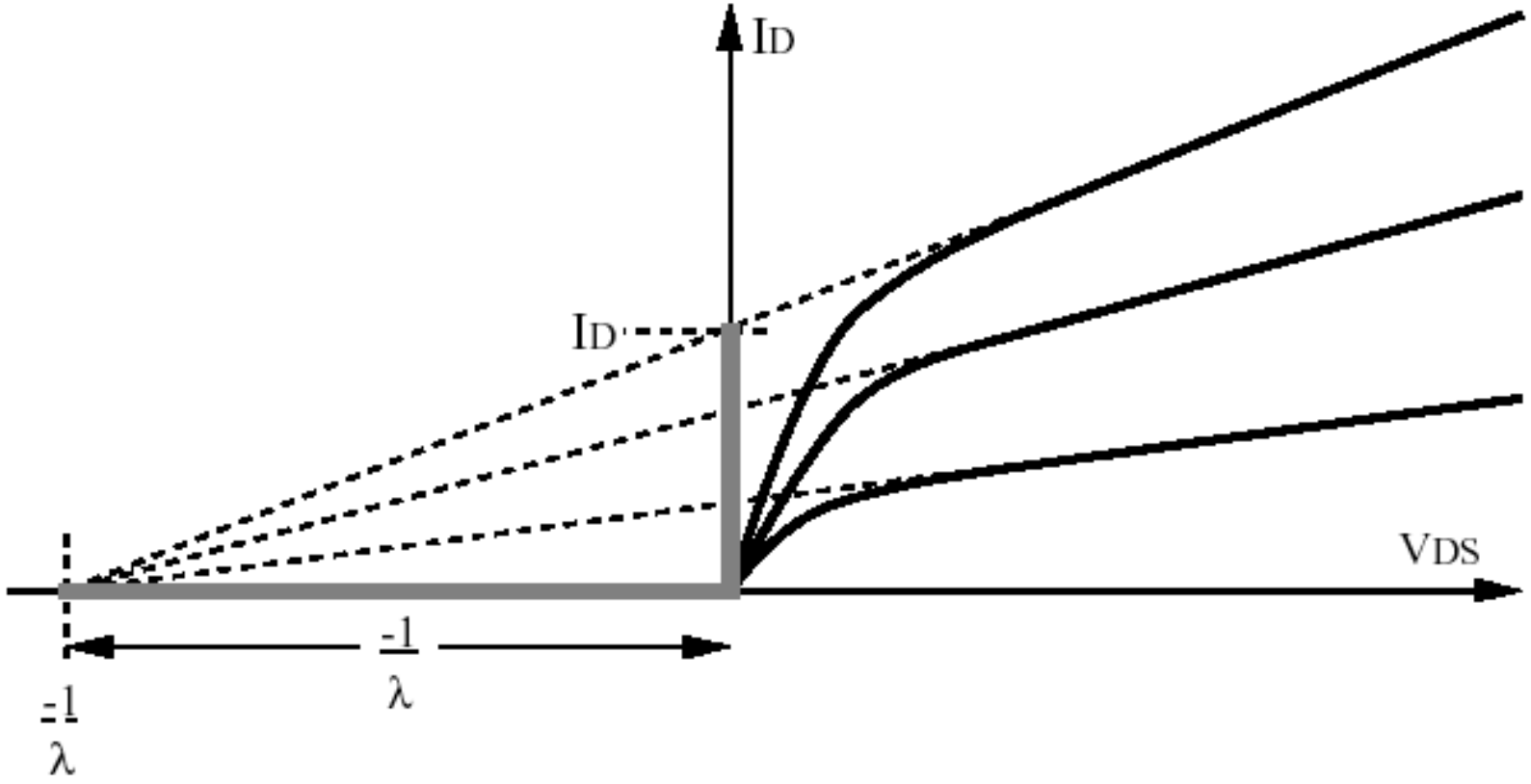

**"Family" of curves**

# $I_D$- $V_{DS}$ Characteristic for Different $V_{GS}$




**Extrapolate backward: intersect at $V_{DS}$-axis**

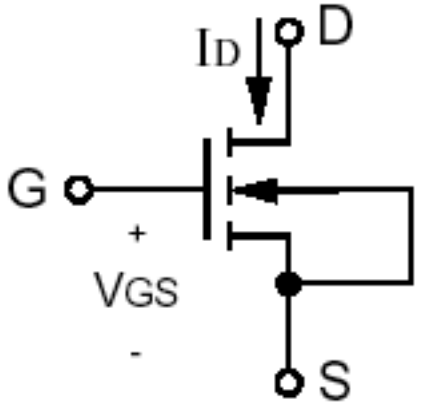
# 1/slope provides small signal resistance $r_o$

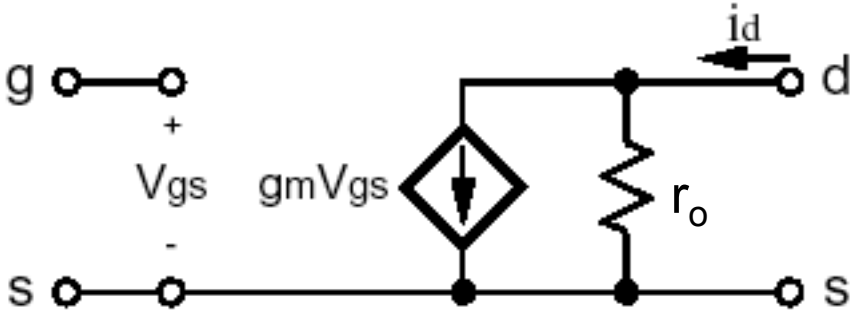



- **Intersect at -1/λ** **Slope:** $\frac{1}{r_o} = \frac{I_D}{1/\lambda} \Rightarrow r_o = \frac{1}{\lambda I_D}$

- **Typical λ values:** **0.01 $V^{-1}$ L > 1$\mu$m**
  **0.2 $V^{-1}$ L < 1 $\mu$m**

# MOSFET small signal model



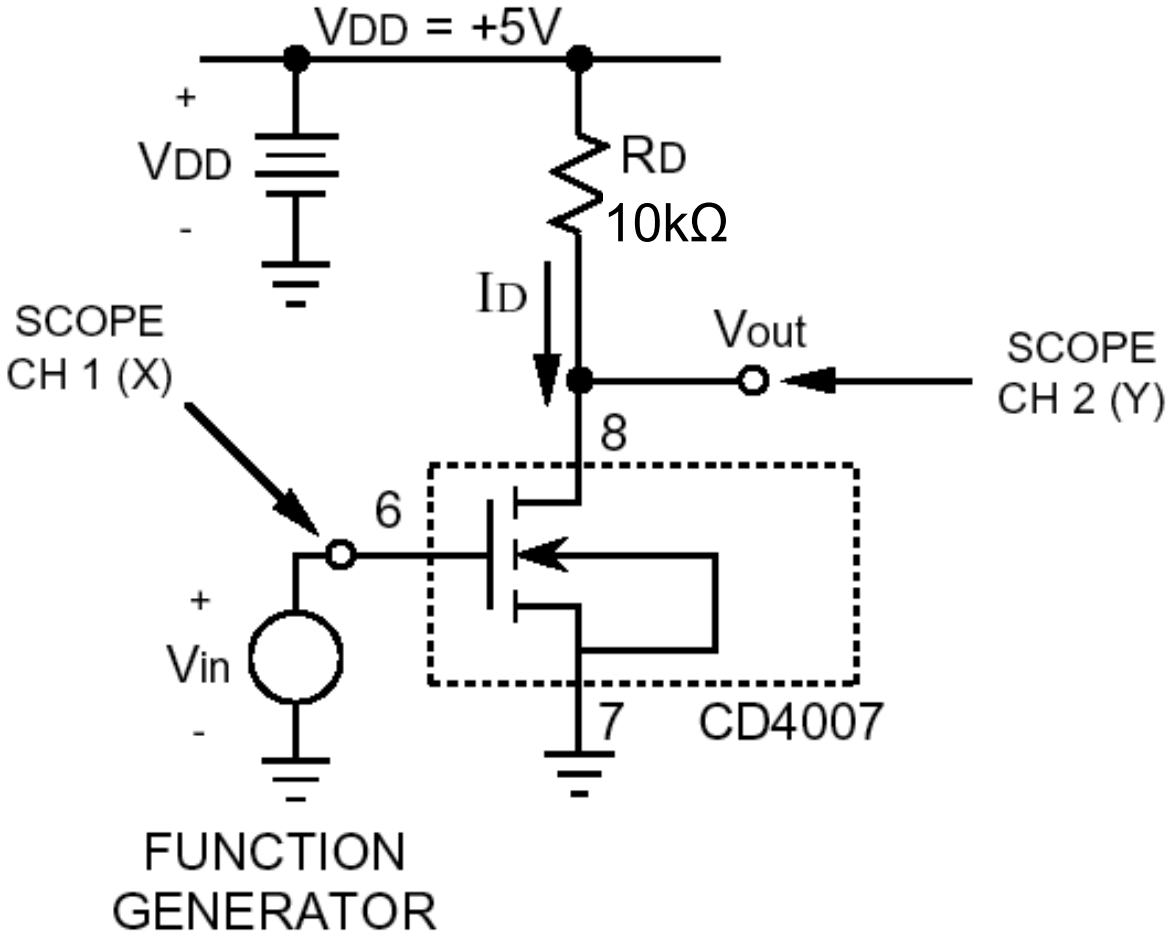

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \qquad r_o = \frac{1}{\lambda I_D}$$

- **$r_o$ in parallel: Model nonideality of current source due to channel length modulation**

# Increasing Gain

- **Typical gain (resistive load)**
  - **Class example: $|A_v| \approx 11.1$**
  - **Lab 4 example: $|A_v| < 10$**
- **How to increase $A_v$?**

# Common source circuit (Lab 4)




**Setting operating point:**

**Adjusted function generator offset for DC output at midpoint of signal swing**

# Common source circuit (Lab 4)

- **DC operating point**
- **Chosen for $V_{OUT}$ halfway between rails**
- **$I_D$=250 $\mu$A**
- **$V_{GS}$ - $V_{TH}$ ≈ 0.5V - 1.0V (depends on parameters)**

$$V_{OUT} = V_{DD} - I_D R_D$$

$$V_{OUT} = +2.5V$$

$$I_D = \frac{V_{DD} - V_{OUT}}{R_D}$$

$$= \frac{5V - 2.5V}{10k\Omega} = 250\mu A$$

# Common source circuit (Lab 4)

- **Small signal gain magnitude ≈ 10**
- **Not impressive!**

$$g_m = \frac{2I_D}{V_{eff}} = \frac{2(250\mu A)}{0.5V}$$

$$g_m = 1.0mA/V$$

$$A_v = -g_m R_D = -(1.0mA/V)(10k\Omega)$$

$$A_v = -10$$

# How to increase $A_v$?

**Look at gain expression:** $A_v = |g_m R_D|$

# Increase $R_D$

- **New $R_D$ = 100kΩ (10X old value)**
- **Problem: DC operating point**
- **Violates condition for saturation region: triode!**
- **DC operating point stuck at negative rail**

$$V_{OUT} = V_{DD} - I_D R_D$$

$$V_{OUT} = 5V - \underbrace{(250\mu A)(100k\Omega)}_{25V}$$

$$V_{OUT} = -20V\ ?$$

# Look at problem symbolically

- Use $g_m = 2I_D/(V_{GS} - V_{TH})$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

- $I_D R_D$ = DC drop on load

$$|A_v| = g_m R_D = \frac{2I_D R_D}{V_{GS} - V_{TH}}$$

- Optimal bias at output: constrained to $V_{DD} / 2$

$$I_D R_D = \frac{V_{DD}}{2}$$

$$|A_v| = \frac{V_{DD}}{V_{GS} - V_{TH}}$$

- $I_D$, $R_D$ not involved!

- Value of approximate symbolic approach vs. "exact" numerical results from simulation

# How to increase gain (resistive load)

- **Increase $V_{DD}$**
  - **usually fixed by application, process**
- **Decrease $V_{GS}$ - $V_{TH}$**
  - **does increase $g_m$**
  - **but area penalty**
  - **Subthreshold for $V_{GS}$ - $V_{TH}$ < 200 mV**

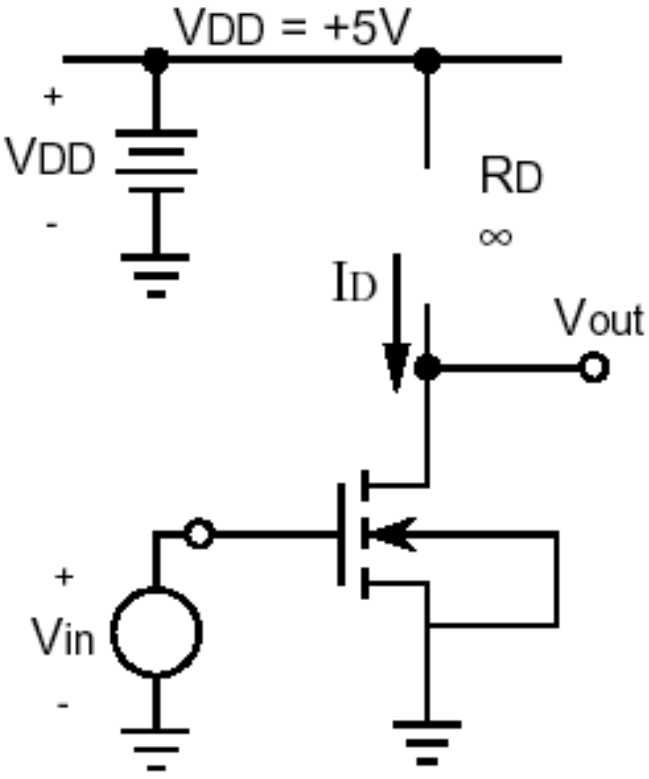
$$|A_v| = \frac{V_{DD}}{V_{GS} - V_{TH}}$$

# Increase $A_v$: Different approach

- **Give up on resistive load ...**
- **What is highest resistance?**

# Increasing $a_v$: Different approach

- What is highest resistance?
- Infinite: open circuit

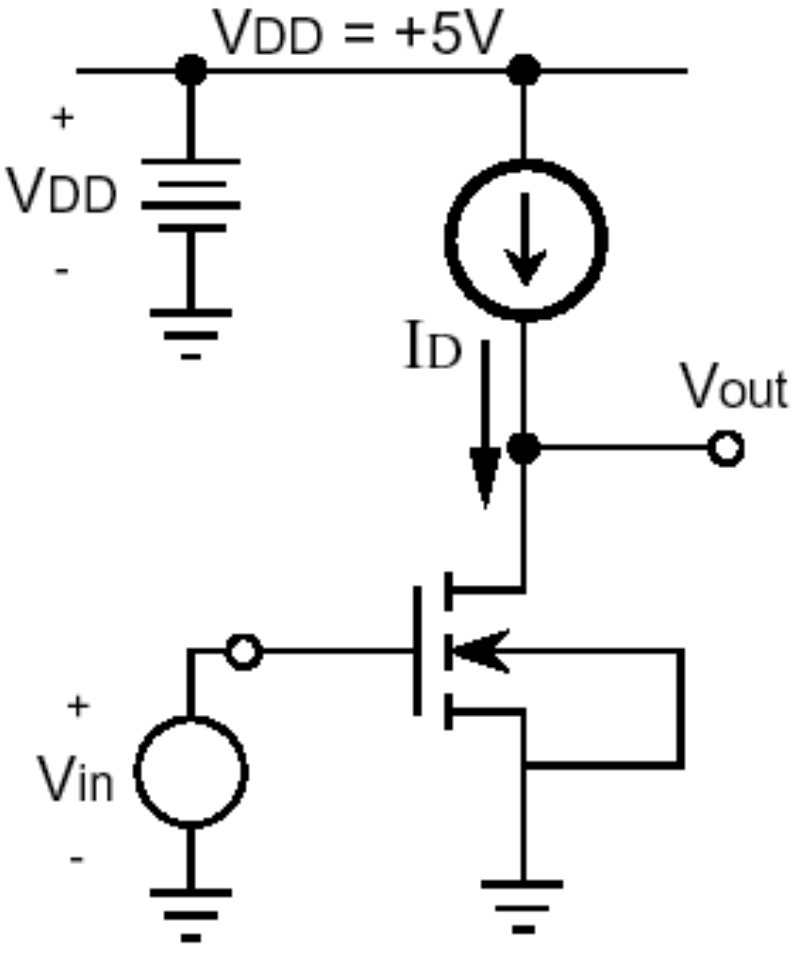



- Problem: no path for $I_D$

- Any circuit element that:
  - provides DC current, but
  - is open circuit in small signal model?

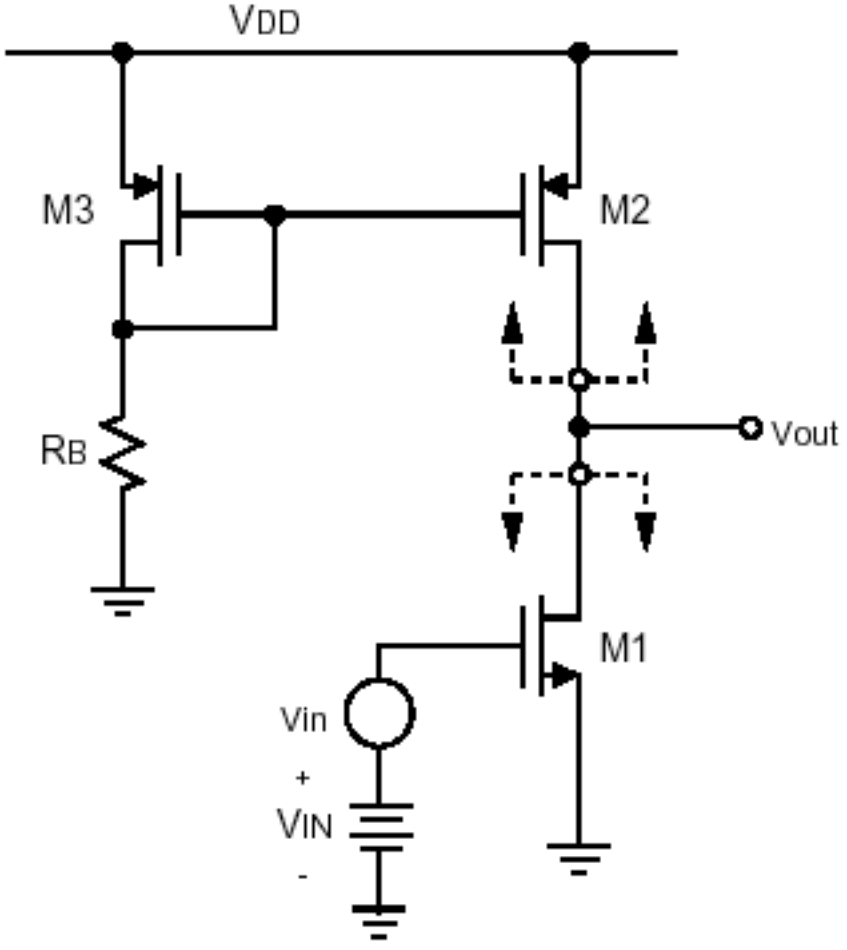
# Current source!

- **Open in small signal model**
- **Realizing current source: MOSFET**



# Lab Circuit: MOSFET with active load

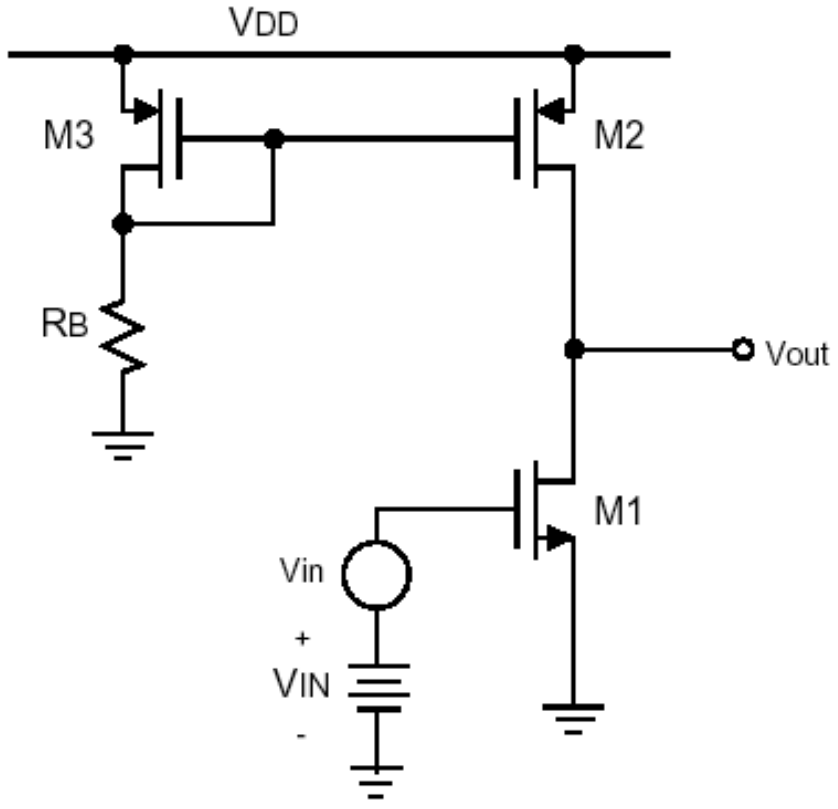
- **Small signal model for M1**
- **Thevenin equivalent "looking into" drain of M2 (see J&M sec. 3.1)**



# Current source load: Large signal considerations

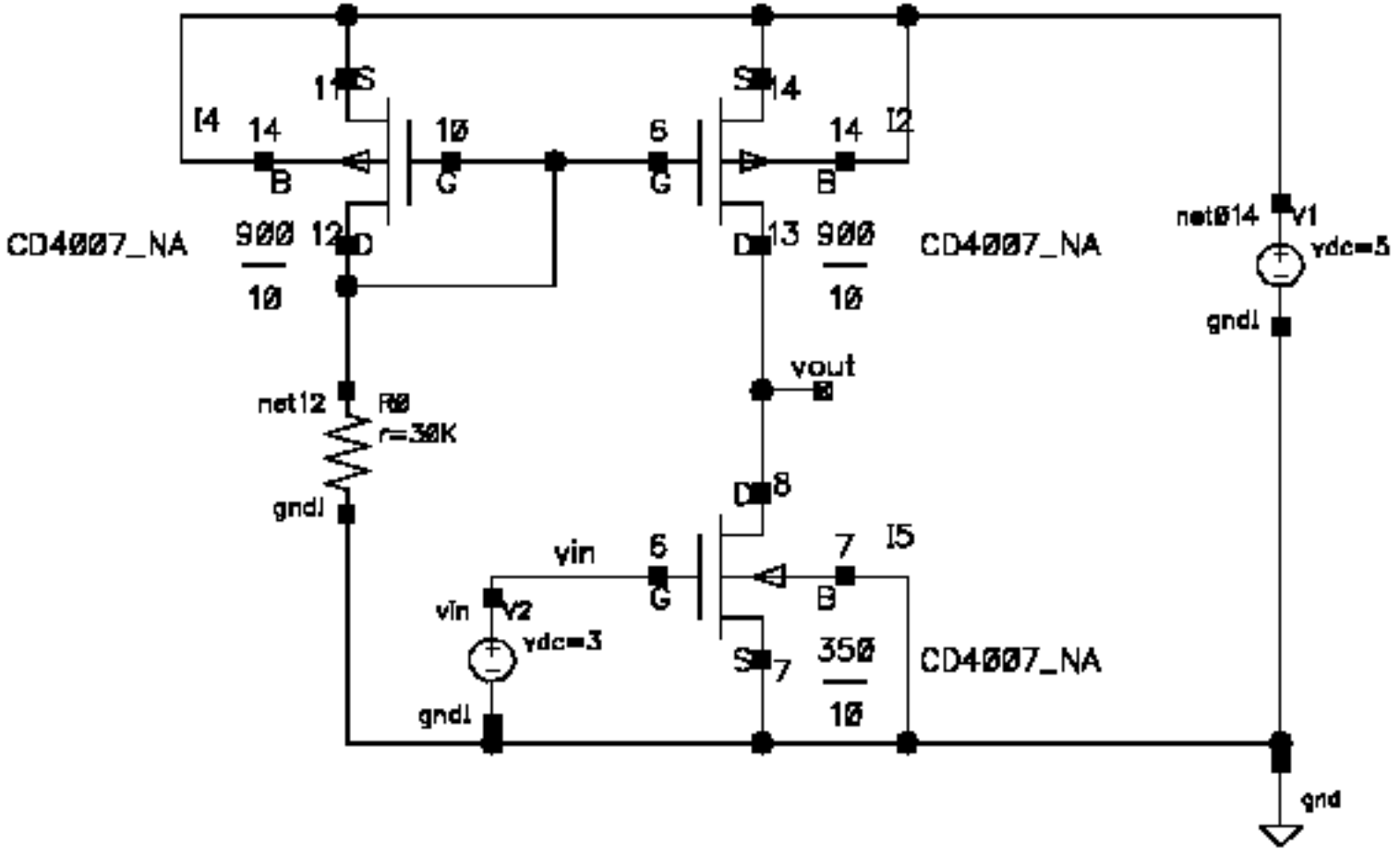
## Output swing limits

- **Top:**
  **M2 "crash" into triode**
- **Bottom:**
  **M1 crash into triode**

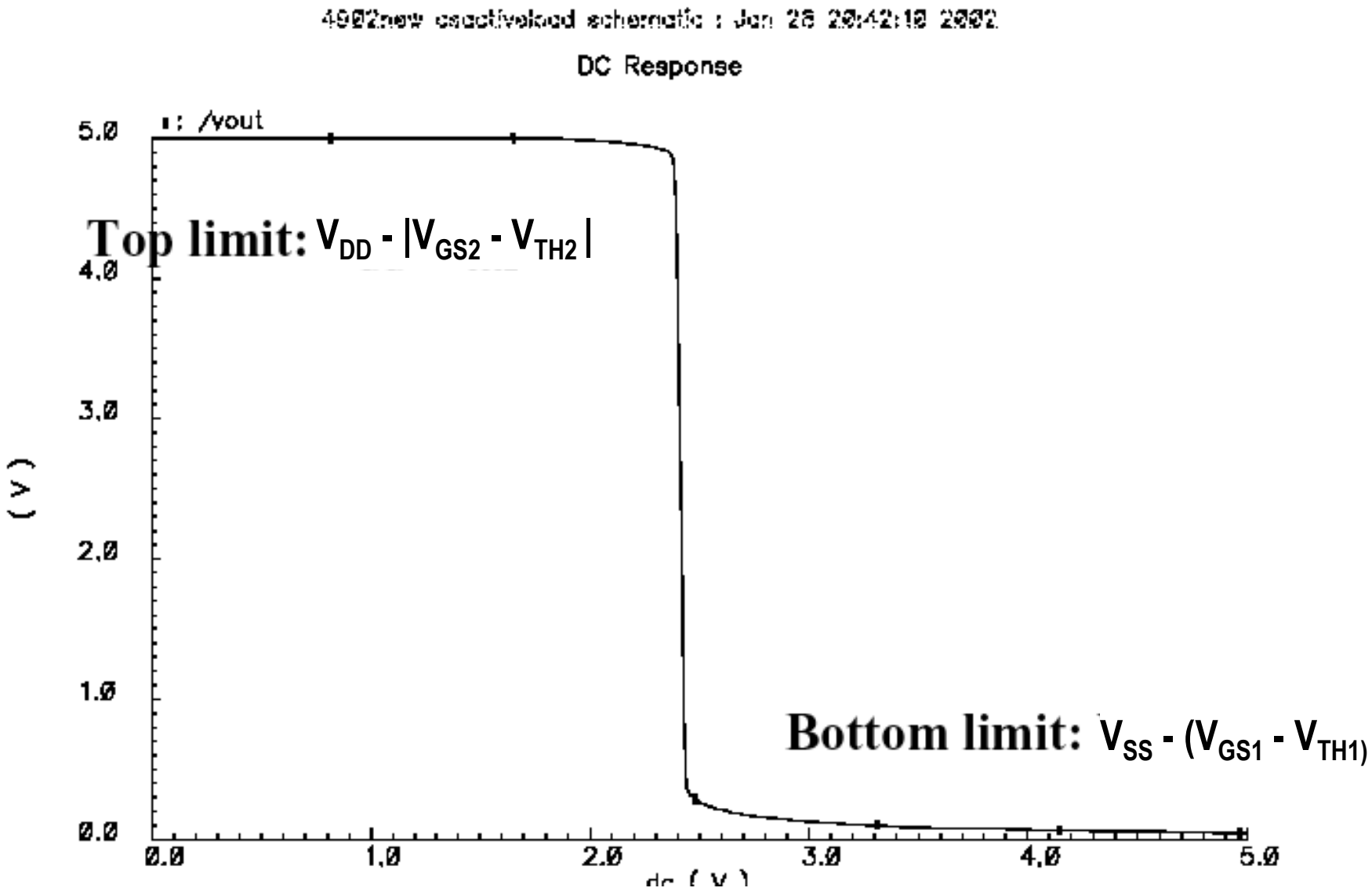


# Common Source with Active Load

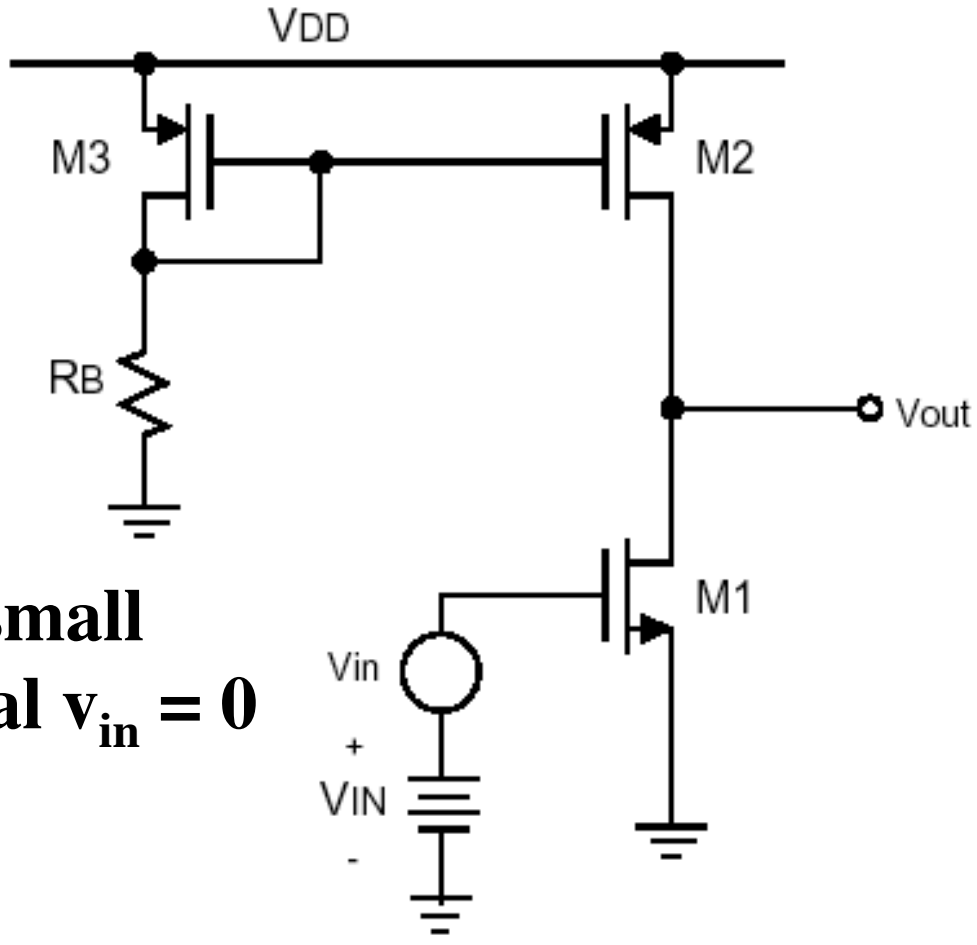
- **DC Sweep Schematic**



# Active Load Simulation Result (DC Sweep)



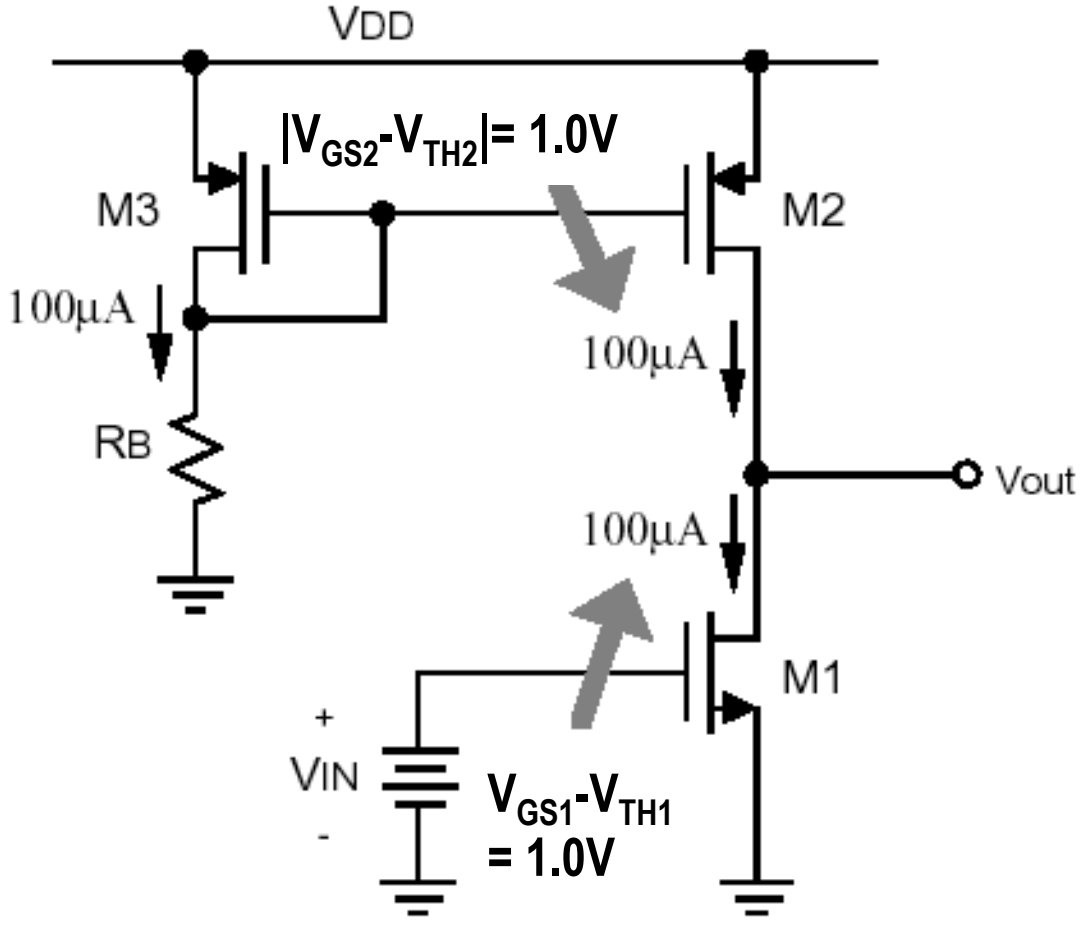
# Determining DC Operating Point




**Set small signal $v_{in} = 0$**

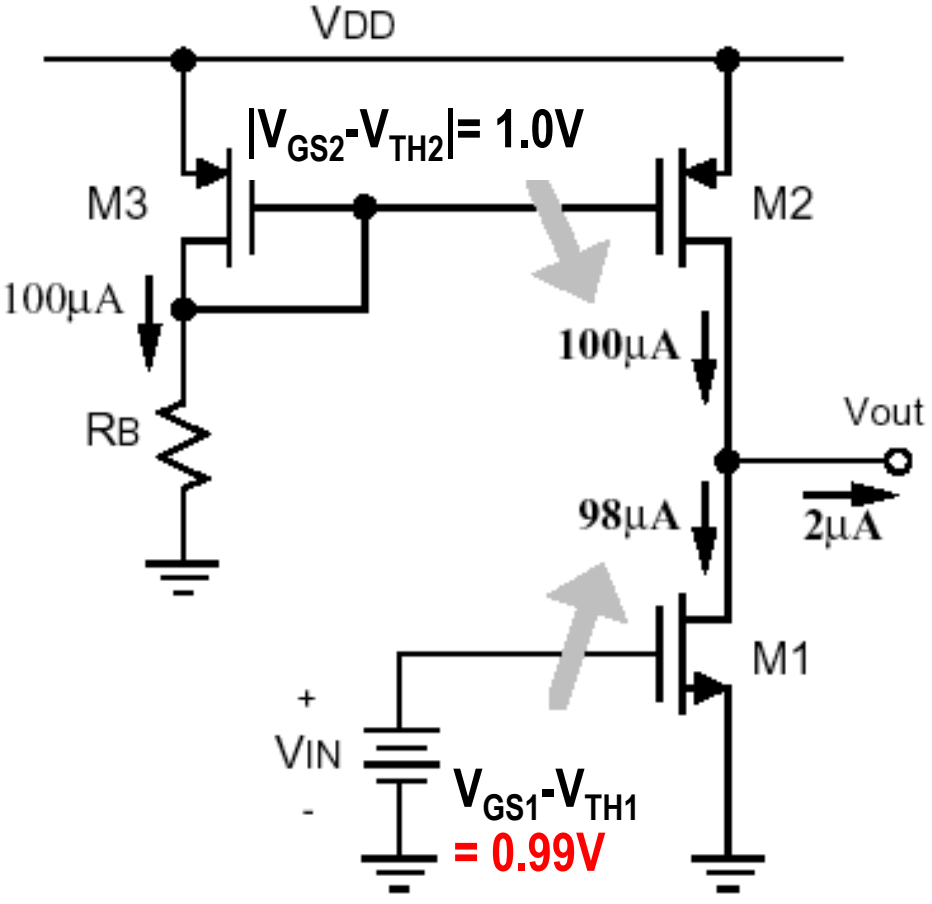
# Determining DC Operating Point

- **Active region: $V_{GS}$-$V_{TH}$ determines $I_D$**
- **Correct $V_{IN}$: M1, M2 "agree"**
- **Example: $V_{GS}$-$V_{TH}$ = 1.0V $I_D$ = 100 $\mu$A**



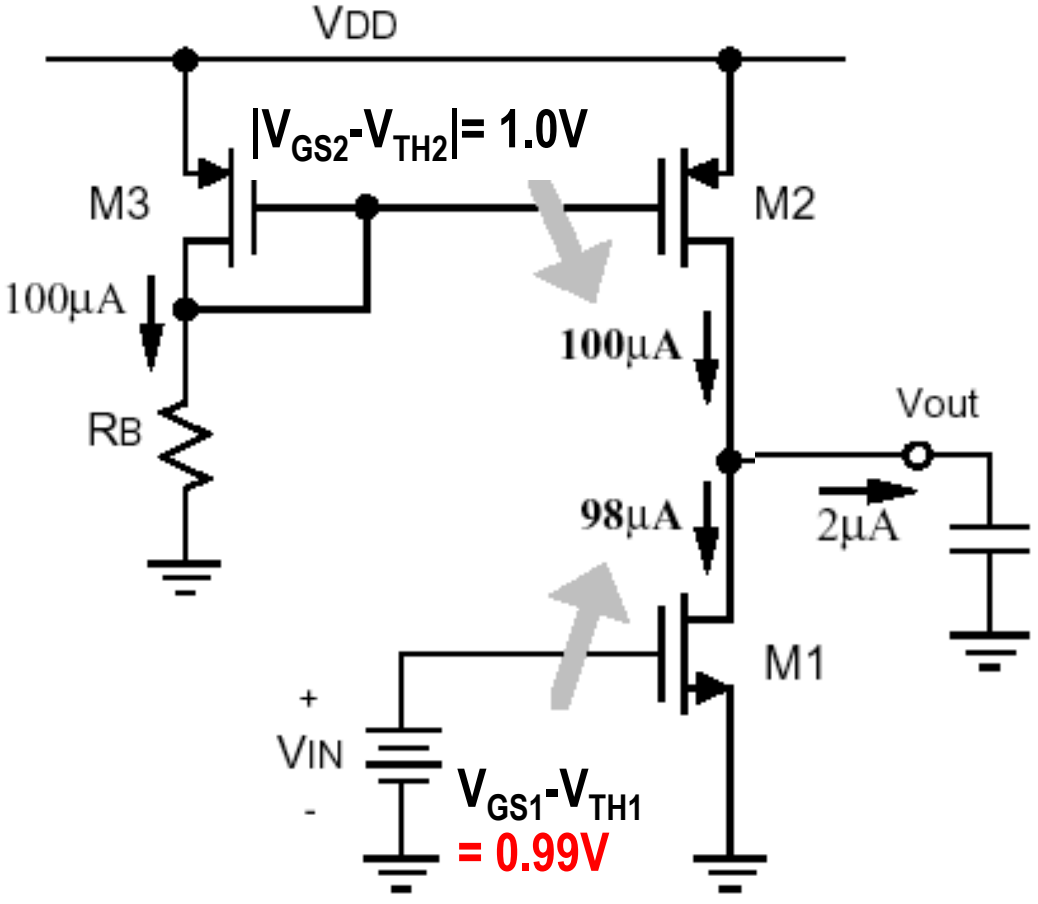
# If DC bias at input is "wrong"?

- **Current source "disagreement"**
- **KCL crisis at output: 2$\mu$A, nowhere to go**
- **What happens?**



# If DC bias at input is "wrong"?

- Capacitance at output node $V_{out}$
- $2\mu A$ flows into cap, charges up:
  - $\Rightarrow V_{DS1}$ increases
  - $\Rightarrow I_1$ increases
  - $\Rightarrow V_{DS2}$ decreases
  - $\Rightarrow I_2$ decreases
- Changes in $V_{DS}$ cause changes in $I_D$ until "agreement" is reached: $I_{D1} = I_{D2}$



# How much change in $V_{DS}$?

- Changes in $V_{DS}$ cause changes in $I_D$ until "agreement" is reached: $I_{D1} = I_{D2}$ BUT
- Saturation: $I_D$ is a weak function of $V_{DS}$
- Large change in $V_{DS}$ for small change in $I_D$
- Output very sensitive to changes in $I_D$:
- Small $\Delta V_{GS}$ at input $\Rightarrow$ Small $\Delta I_D \Rightarrow$ Requires large $\Delta V_{DS}$ at output for $I_D$ agreement

**Good: high voltage gain**

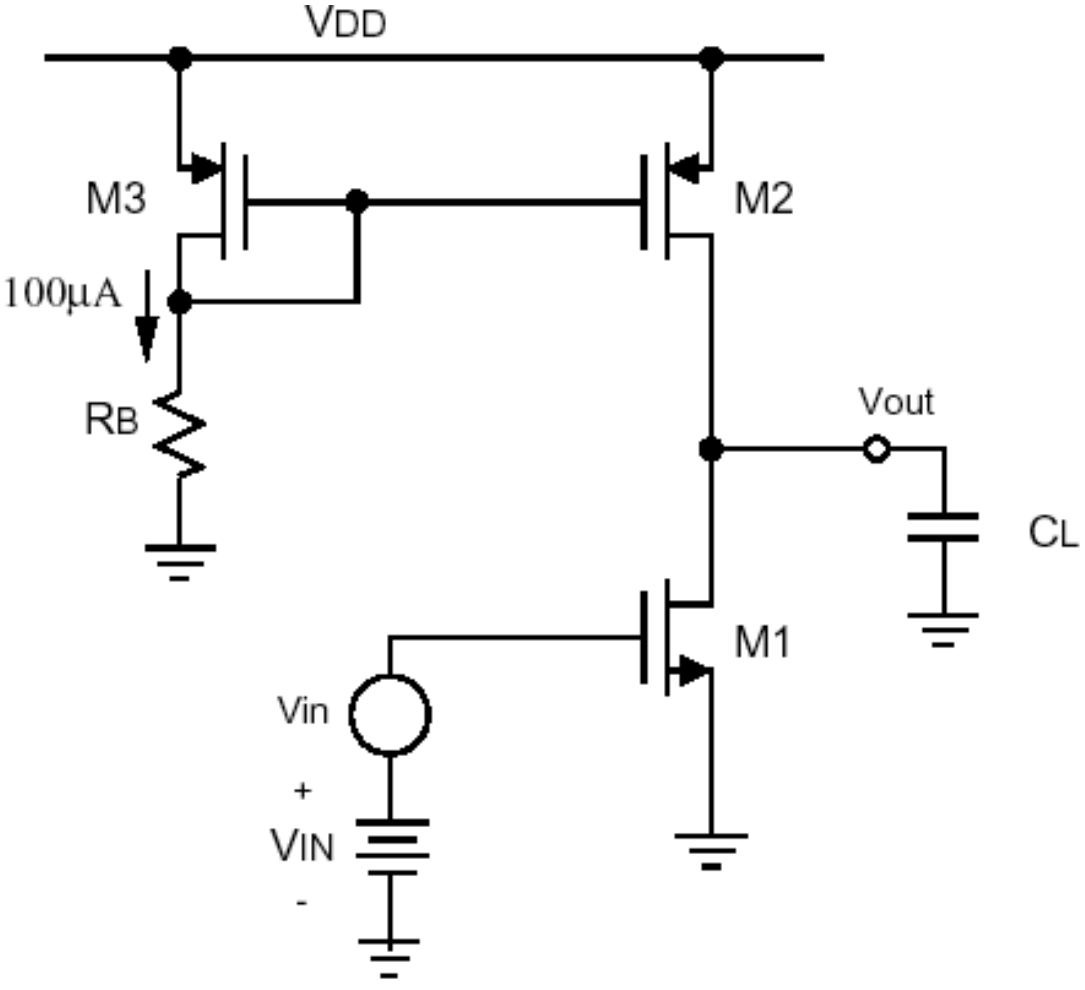
**Bad: tricky to get correct input bias point**

# Frequency Domain Considerations

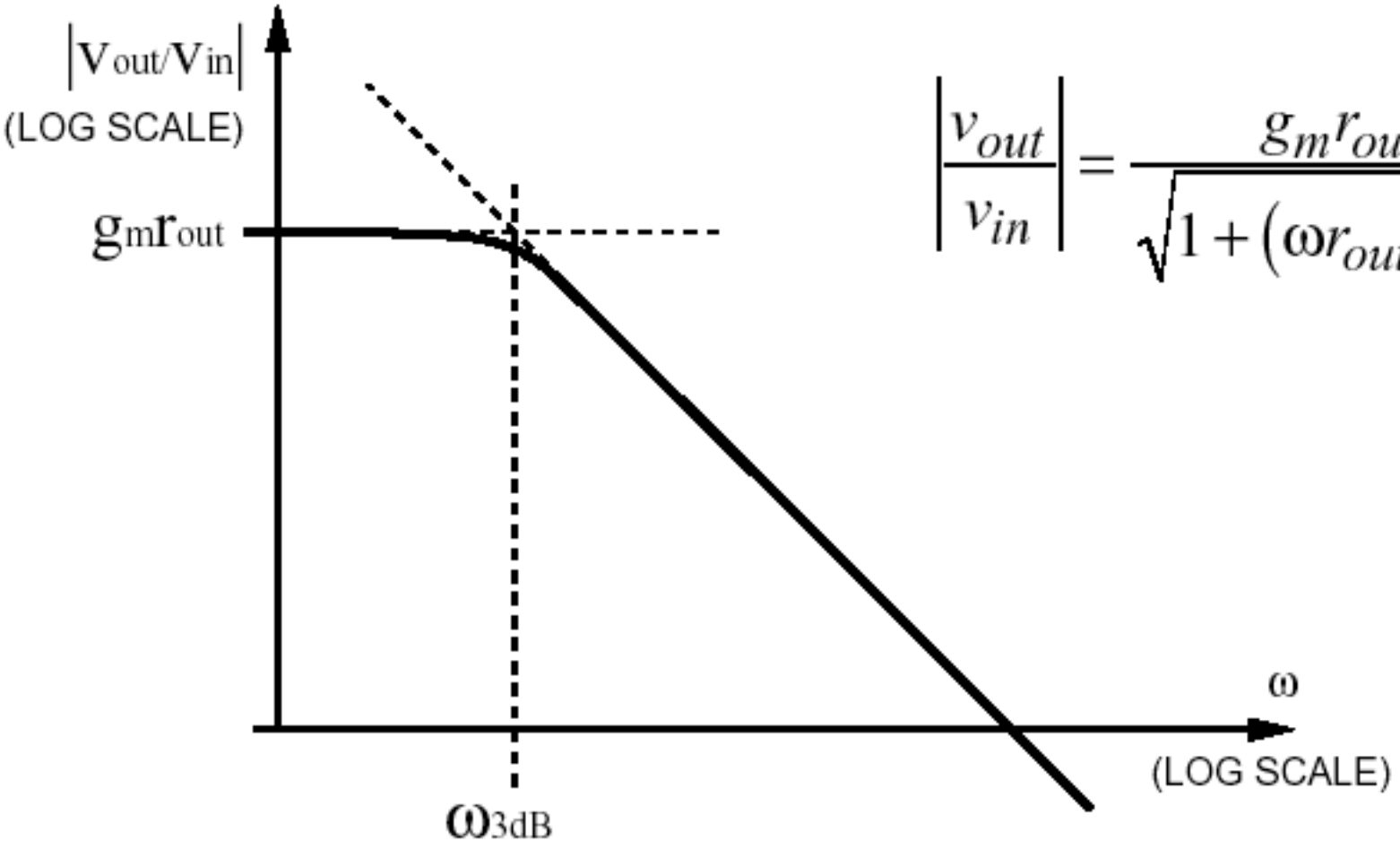
- **Ideal op-amp goals:**
  - **Infinite gain**
  - **Infinite bandwidth**
- **Active load helps gain**
- **What about bandwidth?**

# Frequency Domain Analysis

- **Start simple: Assume single $C_L$ at output**
- **(Ignore MOS capacitances for now …)**
- **Find transfer function $v_{out}/v_{in}$**



# Bode Plot of Transfer Function Magnitude




$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{g_m r_{out}}{\sqrt{1+\left(\omega r_{out} C_L\right)^2}}$$

**Bandwidth: $\omega_{3dB}$**