Name _____

ECE Box # _____

Problem	Score	Points
1	_____	36
2	_____	30
3	_____	16
4	_____	18

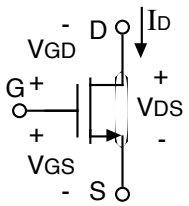
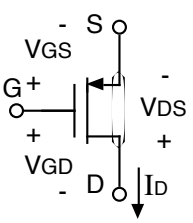
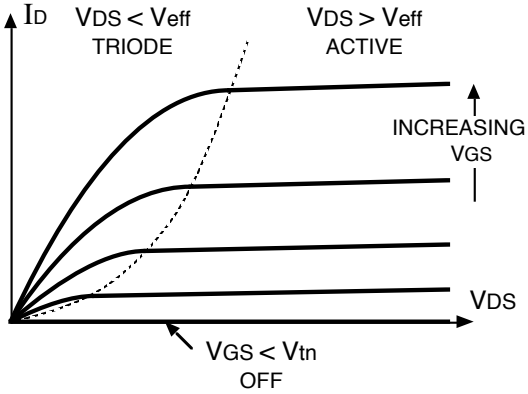
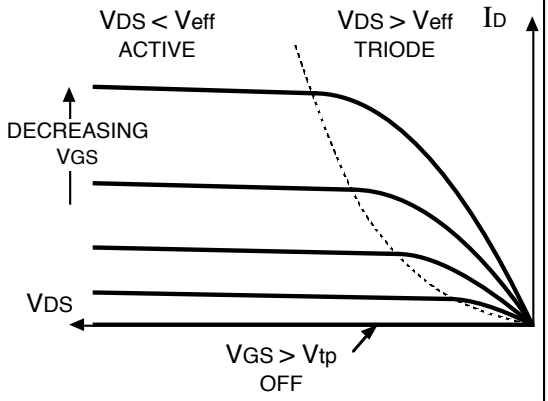
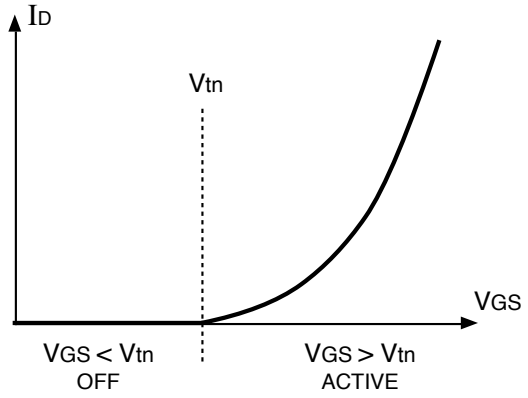
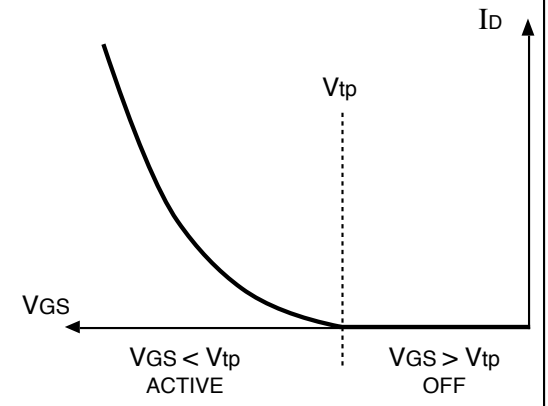
EE4902 C2001

Analog IC Design

Exam 3

- This is a **closed book test!**
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- **Look for the simple, straightforward way to solve the problem for the level of accuracy required. Don't get entangled in unnecessary algebra.**
- You may assume all op-amps to be ideal, except as otherwise noted.
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- You will have 55 minutes to complete this exam. There are four problems on a total of 11 pages.

MOSFET LARGE SIGNAL CHARACTERISTICS

	N CHANNEL	P CHANNEL
CIRCUIT SYMBOL		
ACTIVE	$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \underbrace{(V_{GS} - V_{tn})}_{V_{eff}}^2 [1 + \lambda_n (V_{DS} - V_{eff})]$	$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} \underbrace{(V_{GS} - V_{tp})}_{V_{eff}}^2 [1 + \lambda_p \lvert V_{DS} - V_{eff} \rvert]$
I_D-V_{DS} CHARACTERISTIC		
I_D-V_{GS} CHARACTERISTIC **(ACTIVE REGION)**		
TRIODE REGION	$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2}]$	$I_D = \mu_p C_{ox} \frac{W}{L} [(V_{GS} - V_{tp}) V_{DS} - \frac{V_{DS}^2}{2}]$

1. This problem is concerned with the op-amp circuit shown in Figure 1. The op-amp is connected as a unity gain follower with a 1V DC input. For the purposes of this problem, you may ignore channel length modulation effects and the body effect.

Use the following MOSFET parameters for the AMI 1.2μm process:

Parameter	N-channel	P-channel	Units
V_t	+0.61	-0.83	V
μC_{ox}	7.42E-5	1.93E-5	A/V^2

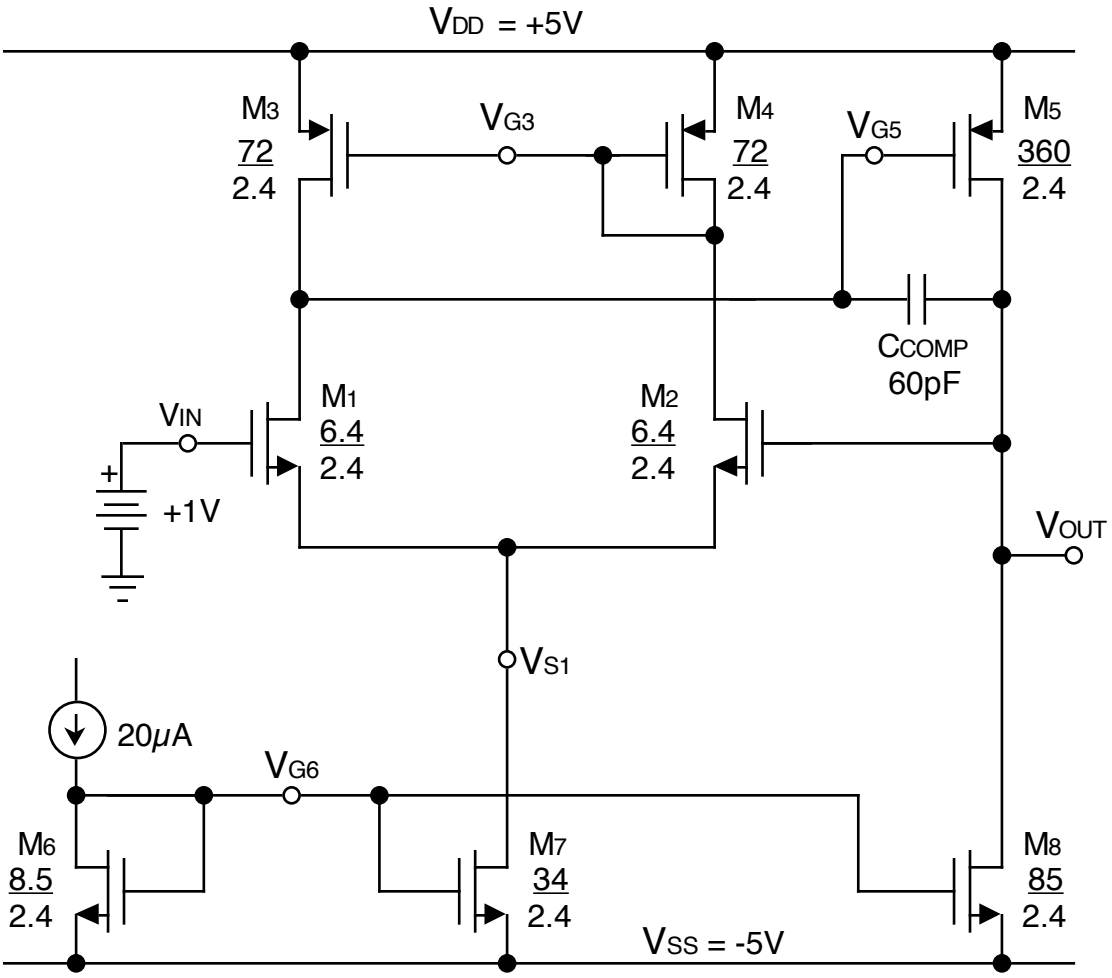


Figure 1a.

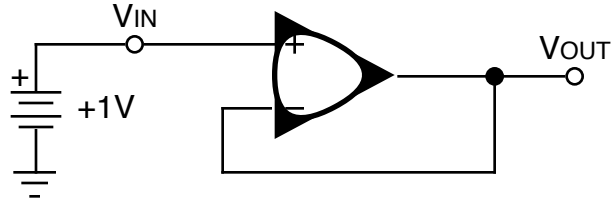


Figure 1b.

a) Find the DC drain current I_D (accuracy ±10%) for all MOSFETs. Use the table below to record your answers.

[12]

	DC Current I_D [μA]
M1	
M2	
M3	
M4	
M5	
M6	
M7	
M8	

b) Find the DC node voltages (accuracy ±50mV) for all nodes. Use the table below to record your answers.

[12]

	Node voltage [V]
V_{IN}	
V_{OUT}	
V_{S1}	
V_{G3}	
V_{G5}	
V_{G6}	

c) Will this op-amp exhibit a systematic offset?

[1]

YES **NO**

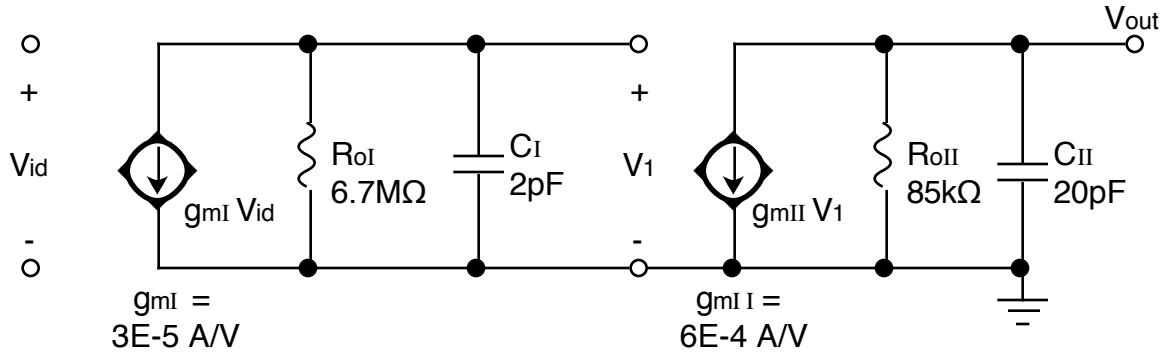
EXPLAIN! **[5]**

d) What is the slew rate (accuracy ±10%) for this op-amp?

[6]

Slew Rate = _____

2. The small-signal model of a two stage op-amp is shown below:



a) Determine the open-loop DC gain A_0 (accuracy ±10%):

[6]

A_0 = _____

b) On the following page, plot the magnitude and phase Bode plots for the open loop gain transfer function $A(f)= v_{out}/v_{in}$.

[12]

c) With feedback for a closed-loop gain of unity, will this op-amp be stable or unstable?

[1]

STABLE **UNSTABLE**

EXPLAIN! **[5]**

NOTE: WHICH PART (d) YOU ANSWER DEPENDS ON YOUR ANSWER TO (c)!!!
ONLY ANSWER ONE OF THE QUESTIONS BELOW!!!

d) **[6]**

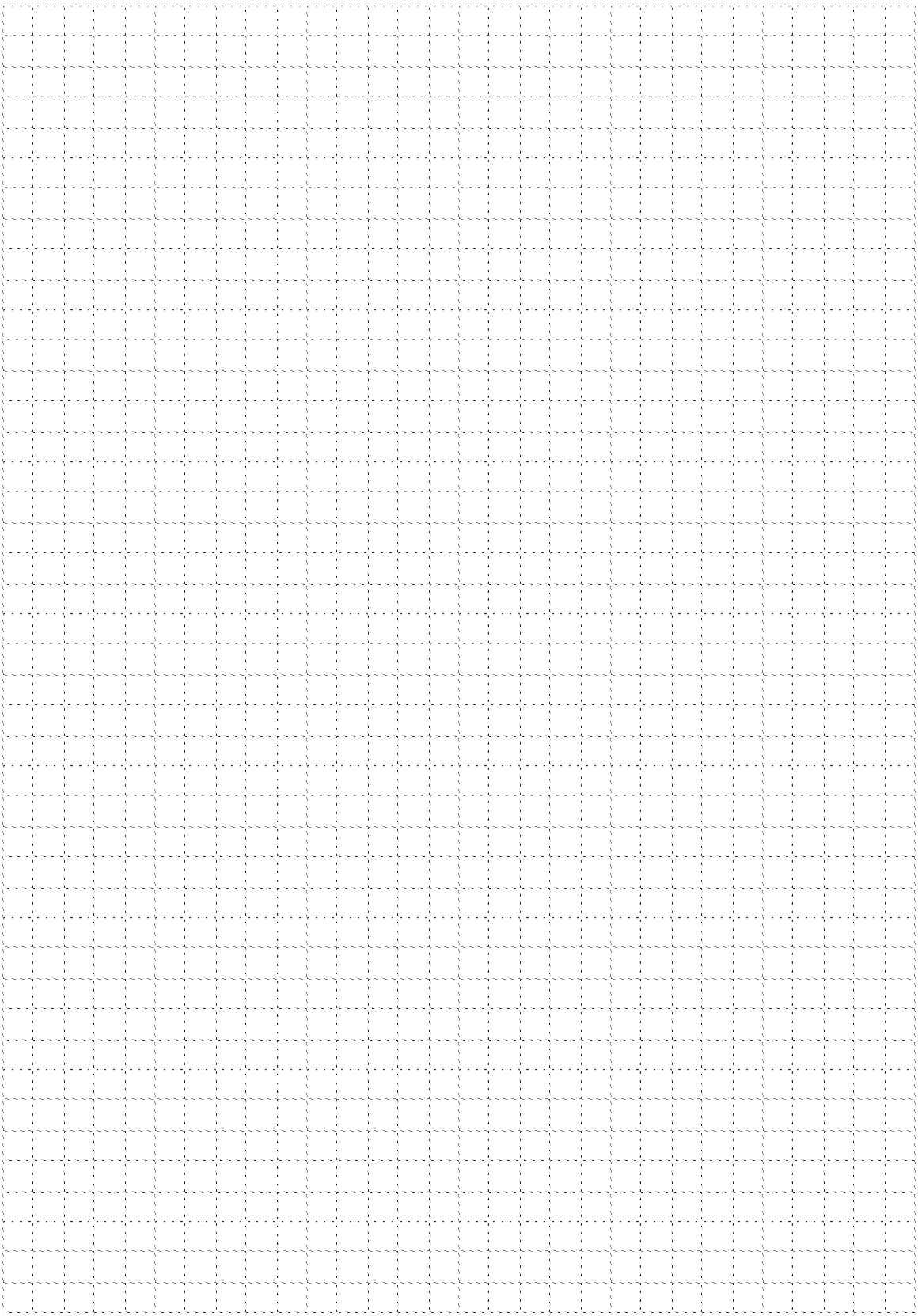
IF YOU SAID STABLE

Determine the gain-bandwidth product f_T:

f_T = _____

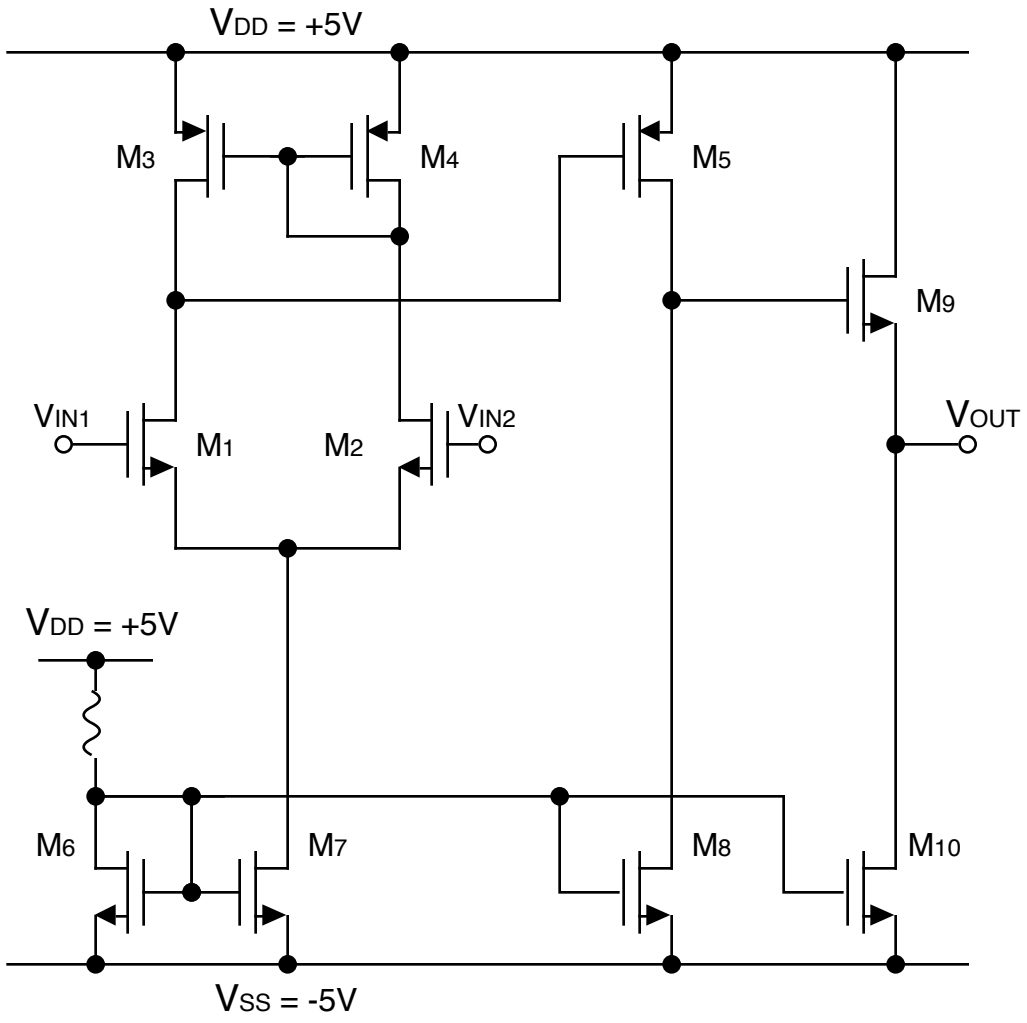
IF YOU SAID UNSTABLE

Describe qualitatively what design change(s) would be necessary to stabilize the op-amp:



3. One problem with the simple two-stage op-amp you built in Lab 3 is the high output impedance. That's why you had to use feedback resistors of 1MΩ and 100kΩ in the gain of +11 amplifier -- lower values would have loaded down the output stage, reducing open-loop gain and drawing too much current.

   One solution to this problem is to add a source follower buffer at the output stage, as shown in the op-amp circuit below (compensation capacitor omitted for simplicity). M9 is the source follower transistor; M10 is a current source to provide DC bias current for M9.



a) Identify the inverting and non-inverting inputs.

[8]

Inverting: _____

Non-inverting: _____

b) The maximum and minimum limits on the input common mode voltage (defined as $V_{ICM} = (v_{IN1} + v_{IN2})/2$) and the output voltage v_{OUT} are determined by the condition that all MOSFETs operate in the active region. As you may recall from lecture, lab, and problem sets, at each limit one transistor "crashes" into the triode region.

This part of the problerm requires no numerical calculation! For each voltage limit case below, just tell which transistor crashing into triode determines the voltage limit.

[8]

Voltage Limit Condition	MOSFET "crashing"
Common mode voltage, maximum (V_{ICM+})	M____
Common mode voltage, minimum (V_{ICM-})	M____
Output voltage, maximum	M____
Output voltage, minimum	M____

4. This problem considers two implementations of a cascode current source, shown in Figs. 4a and 4b. For the purposes of this problem, you may ignore channel length modulation effects and the body effect. Also, assume that all P-channel devices are operating in the active region; this problem is concerned with the N-channel devices making up the cascoded current mirror.

Use the following MOSFET parameters for a typical MC14007:

Parameter	N-channel	Units
V_t	+1.70	V
μC_{ox}	3.5E-5	A/V^2

The "traditional" cascode current source (shown in Fig. 4a) is great for achieving very high small-signal output impedance. Unfortunately, the tradeoff in reduced signal range (due to the compliance voltage limit) is severe. This can be especially troublesome in low-supply-voltage environments, such as with the single +5V supply rail shown in Fig. 4a.

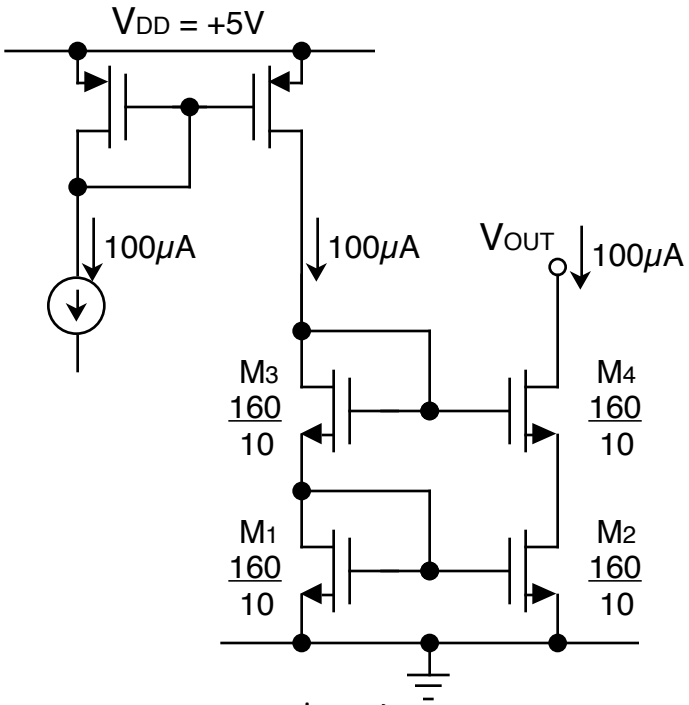


Fig. 4a

a) For the circuit in Fig. 4a, determine the minimum limit $V_{MIN(a)}$ of the voltage compliance range (that is, the minimum voltage at V_{OUT} for which all MOSFETs are in the active region). Accuracy ±50mV.

[6]

$V_{MIN(a)}$ = _____

The problem with the cascode current source shown in Fig. 4a is that the gate of the cascode transistor M4 is set to a higher voltage than it needs to be. M1 and M2 realy do need to be connected in a mirror configuration. But the only purpose of M3 is to set the DC voltage at the gate of M4. We can get better output voltage compliance if we use the approach shown in Fig. 4b.

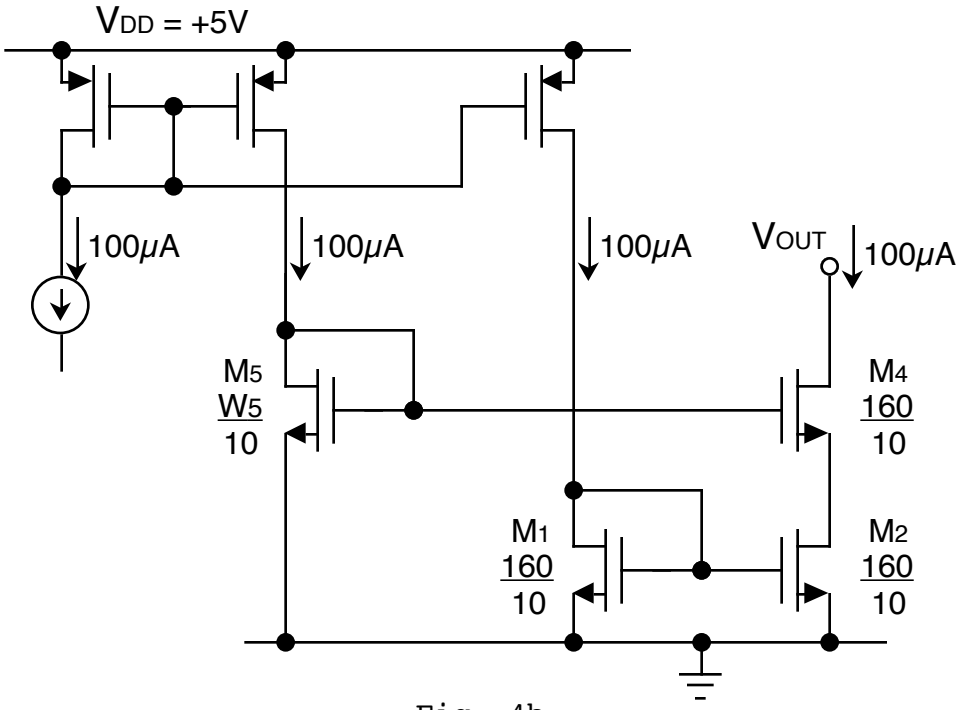


Fig. 4b

b) For the circuit in Fig. 4b, determine the minimum possible limit $V_{MIN(b)}$ of the voltage compliance range (that is, the minimum voltage at V_{OUT} for which all MOSFETs are in the active region) AND the required with W_5 of M5 to achieve this limit.

[12]

$V_{MIN(b)}$ = _____

W_5 = _____