Name SOLUTIONS

ECE Box # _____

A	85-100
B	71-84
C	55-70

MEDIAN 74

μ 73.2

σ 13.9

Problem	Score	Points
1	26.8	30
2	20.2	30
3	13.2	20
4	13.0	20

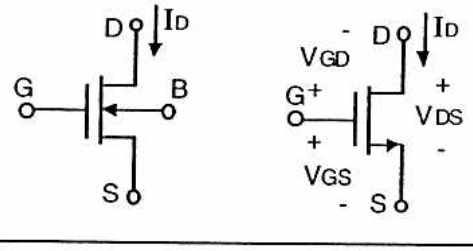
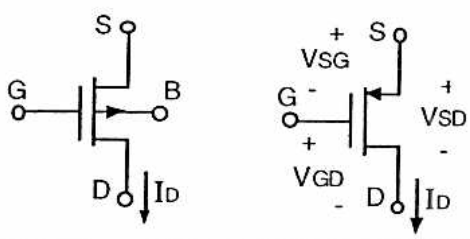
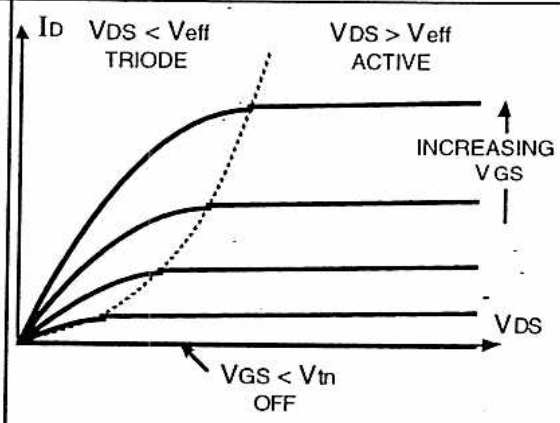
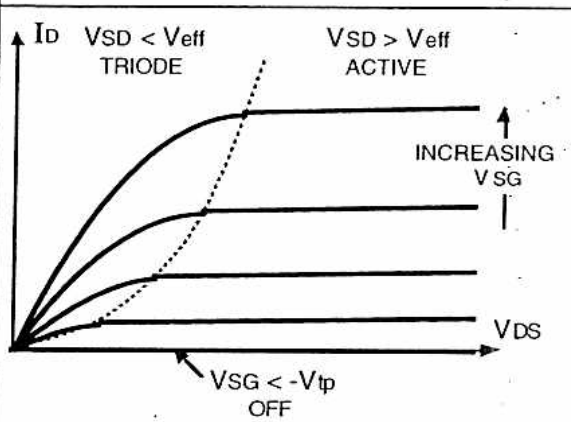
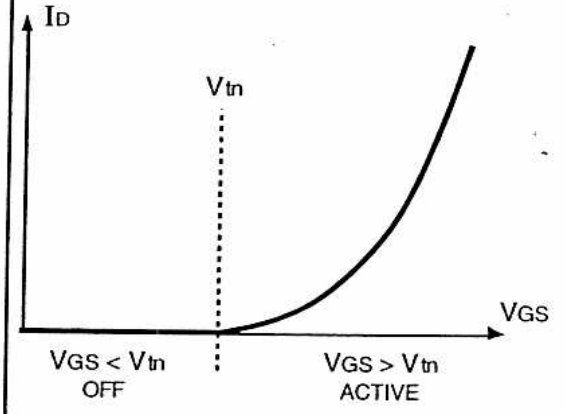
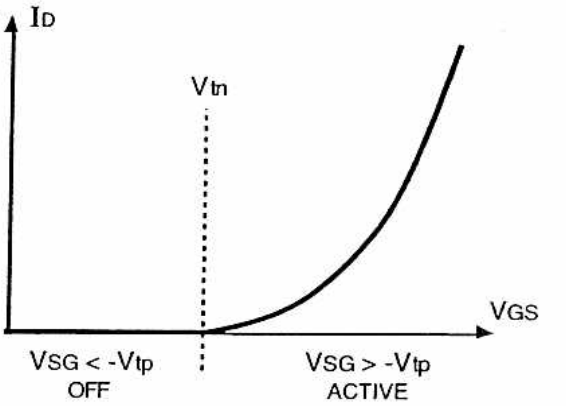
EE4902 C2002

Analog IC Design

Exam 1

- This is a **closed book test**!
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- **Look for the simple, straightforward way to solve the problem for the level of accuracy required. Don't get entangled in unnecessary algebra.**
- You may assume all op-amps to be ideal, except as otherwise noted.
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- You have until 12 noon to complete this exam. There are four problems on a total of 13 pages.

MOSFET LARGE SIGNAL CHARACTERISTICS

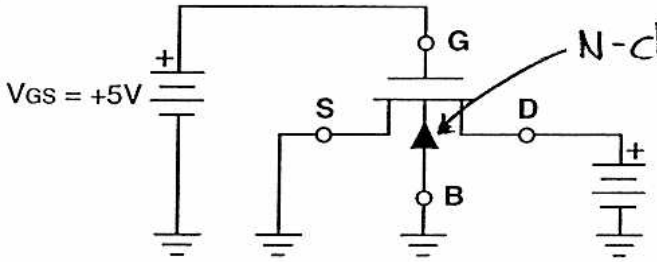
	N CHANNEL	P CHANNEL
CIRCUIT SYMBOL		
ACTIVE	$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \underbrace{(V_{GS} - V_{tn})}_{V_{eff}}^2 [1 + \lambda_n (V_{DS} - V_{eff})]$	$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} \underbrace{(V_{SG} + V_{tp})}_{V_{eff}}^2 [1 + \lambda_p (V_{SD} - V_{eff})]$
I_D-V_{DS} CHARACTERISTIC		
I_D-V_{GS} CHARACTERISTIC (ACTIVE REGION)		
TRIODE REGION	$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2}]$	$I_D = \mu_p C_{ox} \frac{W}{L} [(V_{SG} + V_{tp}) V_{SD} - \frac{V_{SD}^2}{2}]$

1. For each circuit configuration, indicate
   i) the operating region of the MOSFET: cutoff, triode, active
   ii) indicate the dopant type (n or p) in the source, body, and drain regions by writing "n" or "p" in the box in each region on the cross-sectional view of the MOSFET
   iii) sketch the distribution of mobile charge (if any) in the channel under the gate, and indicate if the charge is holes or electrons

$V_{tn} = +1V$ $\quad$ $V_{tp} = -1V$

[10]

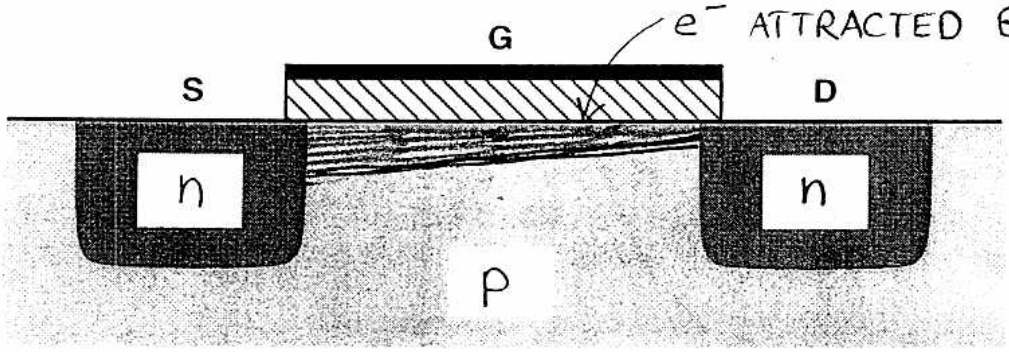
a) Operating Region: CUTOFF (TRIODE) ACTIVE



N-channel, $V_{GS} > V_{tn}$: NOT CUTOFF

$V_{DS} = +1V < V_{eff} = 5V - 1V = 4V$

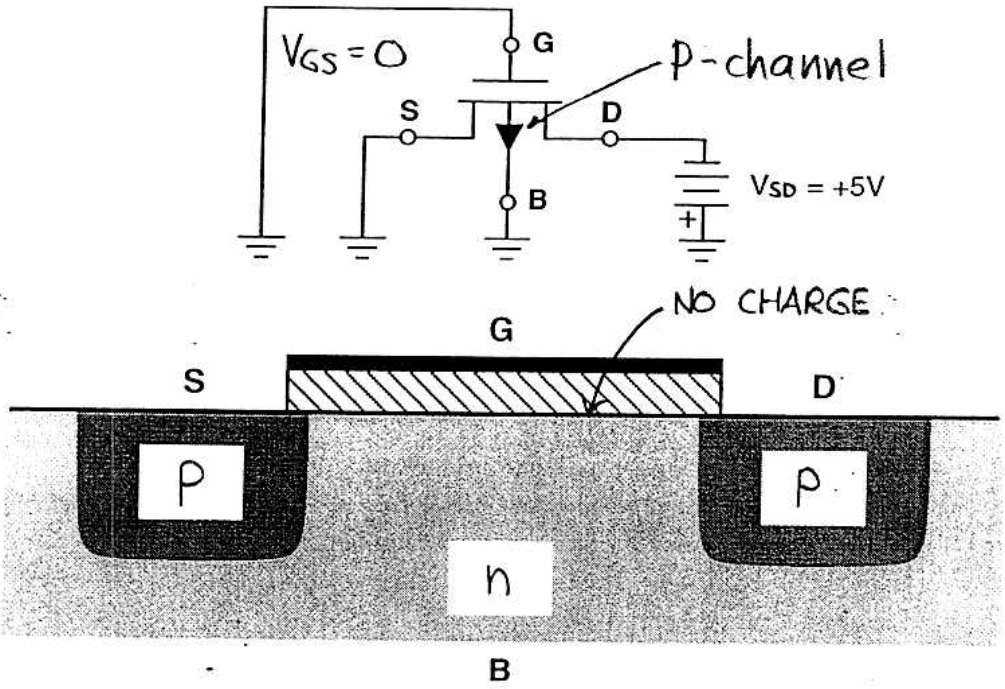
TRIODE



e^- ATTRACTED BY POSITIVE V_{GS}

TRIODE: CHANNEL IS CONTINUOUS FROM S TO D

b) Operating Region: (CUTOFF) TRIODE ACTIVE [10]



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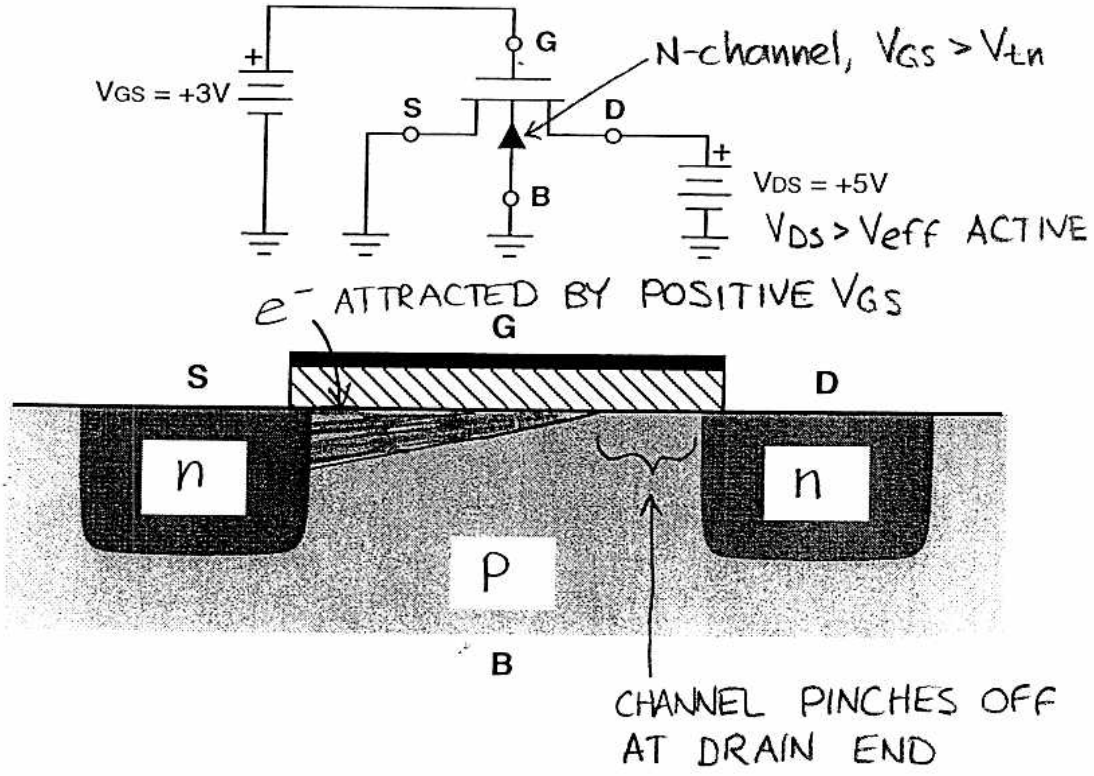
c) Operating Region: CUTOFF TRIODE (ACTIVE) [10]



2. This problem involves design of a circuit both electrically (choosing the input bias voltage) and physically (choosing the MOSFET width) to achieve a desired large signal operating point at the output as well as a specified small signal gain. The circuit is shown in Figure 2a.

You may assume that the substrate (body) terminal is tied to the source terminal. You may also assume channel length modulation to be negligible (λ=0).

Use the following MOSFET parameters for this 2µm process:

Parameter	N-channel	P-channel	Units
V_t	+1.10	-1.20	V
μC_{ox}	5.2E-5	1.5E-5	A/V^2

a) Determine MOSFET width W and input bias voltage V_{BIAS} to achieve an output DC bias level of V_{OUT} = +2.5V and a small signal gain magnitude $|v_{out}/v_{in}|$=10. **[12]**

W = 38.5µm

V_{BIAS} = +1.60V

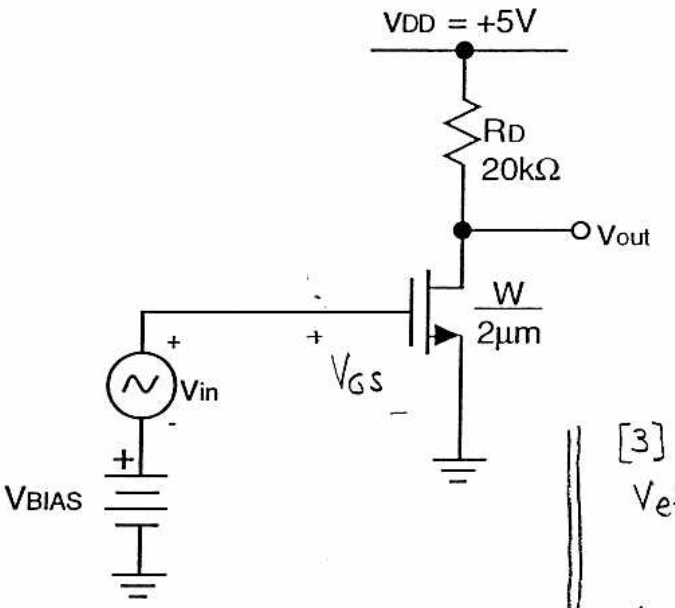


Figure 2a.

DC BIAS

$V_{OUT} = V_{DD} - I_D R_D$

$2.5V = 5V - I_D\, 20k\Omega$

$I_D = \frac{2.5V}{20k\Omega} = 125\mu A$ [1]

SMALL SIGNAL

$\left|\frac{V_{out}}{V_{in}}\right| = g_m R_D$

$10 = g_m (20k\Omega) \Rightarrow g_m = \frac{10}{20k\Omega} = 500\mu A/V$ [2]

FOR g_m, USE

$g_m = \frac{2I_D}{V_{eff}}$

WITH [2]

$\frac{500\mu A}{V} = \frac{2(125\mu A)}{V_{eff}}$

$V_{eff} = 0.5V$ [3]

[3] GIVES V_{BIAS}

$V_{eff} = \underbrace{V_{BIAS}}_{V_{GS}} - V_{tn}$

$V_{BIAS} = V_{eff} + V_{tn} = 0.5V + 1.1V$

$V_{BIAS} = +1.60V$

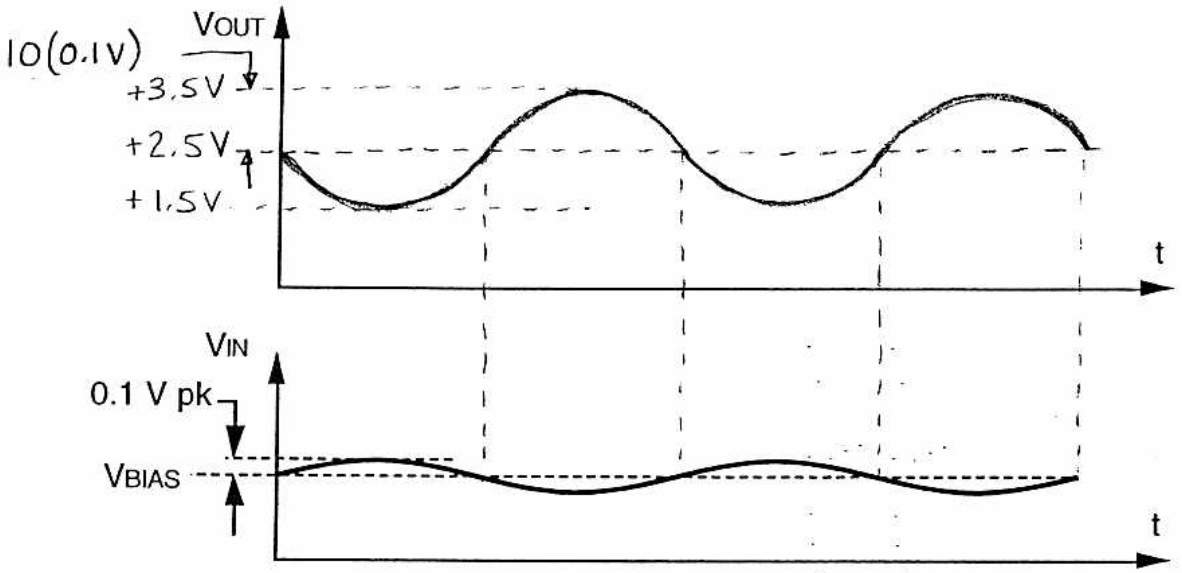
FOR W, USE [1], [3] IN SQ LAW

$125\mu A = \frac{5.2E\text{-}5}{2}\frac{W}{2\mu m}(0.5V)^2$

W = 38.5µm

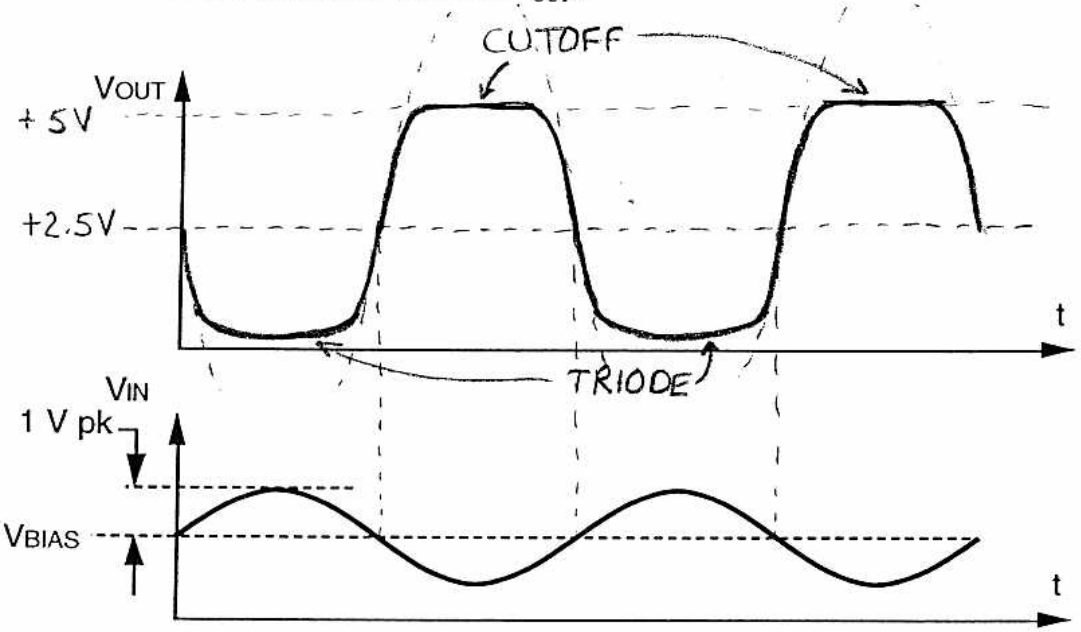
b) Using the axes below, sketch the total output v_{OUT} when v_{in} is a 0.1V peak sine wave. Be sure to indicate numerical values for any interesting voltage levels (for example, approximate maximum and minimum values of v_{OUT}).

[6]



c) Using the axes below, sketch the total output v_{OUT} when v_{in} is a 1V peak sine wave. Be sure to indicate numerical values for any interesting voltage levels (for example, approximate maximum and minimum values of v_{OUT}).

[6]



TOTAL OUTPUT IS SUM OF DC BIAS + (SMALL SIG GAIN)(Vin)
UNLESS RAILS EXCEEDED (EXCEED SMALL SIGNAL LIMIT)

MORE ON THE NEXT PAGE!!!

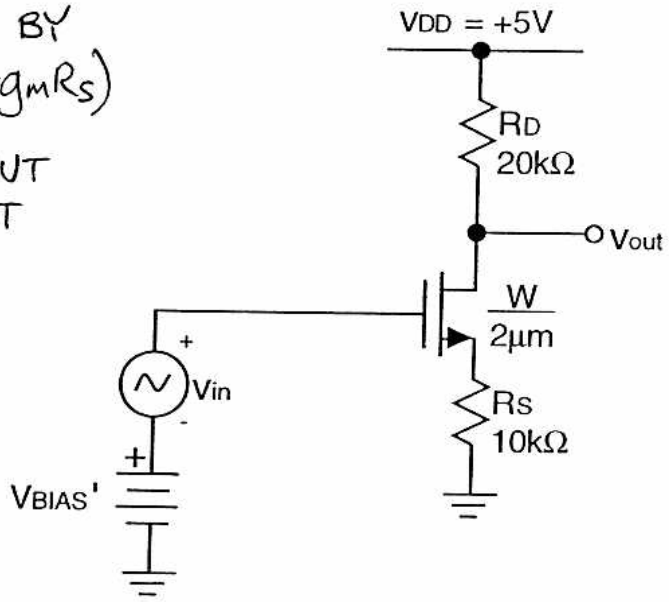
d) Your design from part (a) is modified by inserting resistor R_S in series with the source, as shown in Figure 2b. With the same MOSFET width W, V_{BIAS} is adjusted to a new value V_{BIAS}' so that the DC operating point at the output remains the same and the MOSFET is still in the active region. Will the small-signal gain decrease, remain the same, or increase? [1]

DECREASE **REMAIN THE SAME** **INCREASE**

EXPLAIN! [5]

REDUCED BY FACTOR $(1+g_mR_S)$

KVL AROUND INPUT SHOWS THAT NOT ALL OF V_{in} DROPS ACROSS V_{gs} ⇒ LESS V_{gs} ⇒ LESS g_mV_{gs} ⇒ LESS i_d ⇒ LESS V_{out}

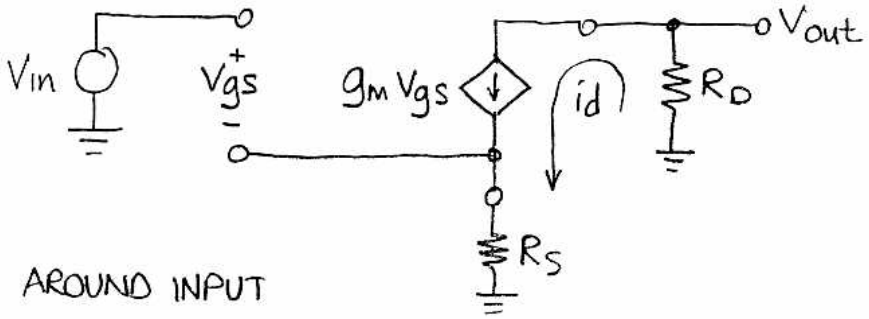


SINCE DC OP PT. AT OUTPUT IS THE SAME, I_D IS THE SAME ⇒ SAME I_D ⇒ SAME W ⇒ SAME V_{eff} ⇒ SAME g_m

BUT GAIN IS REDUCED FROM g_mR_D DUE TO EFFECT OF R_S

Figure 2b.

LOOK AT SMALL SIGNAL MODEL



KVL AROUND INPUT

$V_{in} - V_{gs} - \underbrace{g_mV_{gs}}_{i_d} R_S = 0 \Rightarrow V_{in} = (1+g_mR_S)V_{gs}$ [4]

KVL AROUND OUTPUT

$V_{out} = \underbrace{-g_mV_{gs}}_{i_d} R_D \Rightarrow V_{out} = (-g_mR_D)V_{gs}$ [5]

[5] DIVIDED BY [4]

$$\frac{V_{out}}{V_{in}} = \frac{(-g_mR_D)V_{gs}}{(1+g_mR_S)V_{gs}}$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_mR_D}{1+g_mR_S}$$

3. In most of the op-amp circuits you've worked with so far, you have probably used dual power supplies - for example, the +15V and -15V supply rails in most of the labs in EE3204 (Microelectronics II). This is convenient for processing analog signals: since ground-referenced voltages are located midway between the clipping limits imposed by the supply rails, the undistorted signal swing is maximized for symmetric signals such as sine waves.

The situation is less pleasant in single-supply systems such as we have been considering in EE4902. With only a single supply equal to +5V, the clipping limits are approximately 0V and +5V. Therefore, for maximum signal swing, it's convenient to reference signals to a voltage at +2.5V, midway between clipping limits at the rails. This problem is concerned with the relative merits of two circuits which can be used to develop a "half-supply" voltage midway between the rails.

While a resistive voltage divider might seem attractive, we will see later on in the course that (for die area and power consumption reasons) a "MOSFET-only" approach is better. Two circuits you are considering are shown as options A and B in Figure 3 on the facing page. Option A uses two N-channel devices; option B uses an N-channel and a P-channel.

You may assume that the substrate (body) terminal is tied to the source terminal. You may also assume channel length modulation to be negligible (λ=0)

Use the following MOSFET parameters for this 2µm process AT ROOM TEMPERATURE:

Parameter	N-channel	P-channel	Units
V_t	+1.10	-1.20	V
μC_{ox}	5.2E-5	1.5E-5	A/V^2

a) In each case, find values for the device widths to meet the following requirements: **[10]**

$V_{OUT} = +2.5V$ AND $I_D = 100\mu A$

Indicate your design values in the spaces provided underneath each option

b) Now, consider how each circuit behaves in the presence of variations in threshold voltage due to variations in temperature and fabrication process. Over temperature and process variations, it is observed that the N-channel threshold voltage V_{tn} can vary in a range from +0.9V to +1.3V. It is also observed that the P-channel threshold voltage V_{tp} can vary in a range from -1.05V to -1.35V. It is further observed that these variations are independent, since the N-channel threshold voltage V_{tn} and the P-channel threshold voltage V_{tp} are determined by separate processing steps.

In the presence of temperature and supply variations, which circuit will do a better job of maintaining V_{OUT} equal to +2.5V? Will A be better, B better, or will there be no difference? (Circle one below) **[1]**

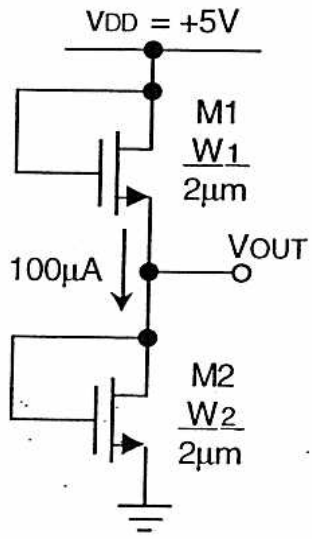
A BETTER **NO DIFFERENCE** **B BETTER**

EXPLAIN! **[9]**

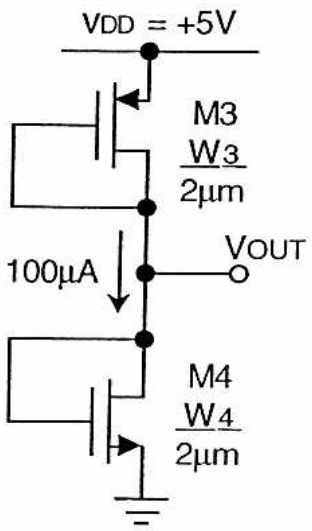
M_1, M_2 IDENTICAL; I_D SAME FOR BOTH $\Rightarrow$ SAME V_{GS}

FOR B: $V_{GS4} = V_{tn} + \sqrt{\frac{\mu_n C_{ox}}{2}\frac{W_3}{L_3}}$ $V_{SG5} = V_{tp} + \sqrt{\frac{\mu_p C_{ox}}{2}\frac{W_4}{L_4}}$

V_{OUT} FOR B DEPENDS ON BOTH V_{tn} V_{tp} WHICH WILL NOT MATCH



A



B

Figure 3.

a) W1 = 3.9µm W2 = 3.9µm

$V_{GS} = 2.5\,V$

USE SQUARE LAW

$100\mu A = \frac{5.2E\text{-}5}{2}\frac{W_1}{2\mu m}(2.5V - 1.1V)^2$

$W_1 = 3.9\mu m$

W3 = 15.8µm W4 = 3.9µm

W_4 WILL BE SAME AS (A)

SQUARE LAW FOR M_3

$100\mu A = \frac{1.5E\text{-}5}{2}\frac{W_3}{2\mu m}(2.5V - 1.2V)^2$

$W_3 = 15.8\mu m$

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b): Over temp & process changes, the current in both circuits will change. B's current may be more or less stable. But for this application we care about the voltage.

4.- You are attempting to design analog circuitry on a digital IC being fabricated in a CMOS process with very short gate length (L=0.18μm). The I_D vs. V_{GS} plot for a MOSFET in the active region (measured using the circuit shown in Fig. 4a) is shown below. The characteristic exhibits a "short-channel" effect: due to velocity saturation of carriers in the channel, the mobility relationship does not hold and the square law equation does not apply for predicting drain current I_D.

$SO\ \frac{2I_D}{V_{eff}} = g_m$ DOESN'T APPLY!

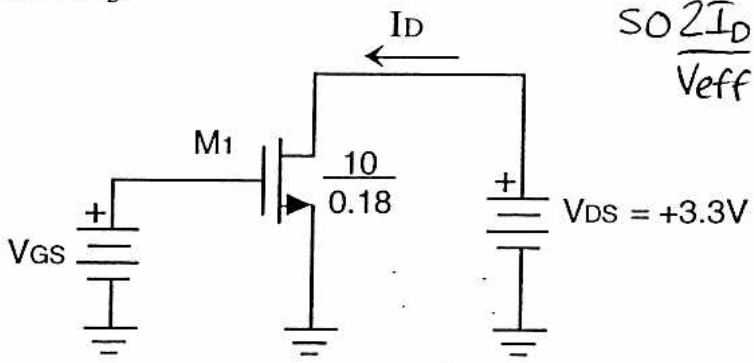
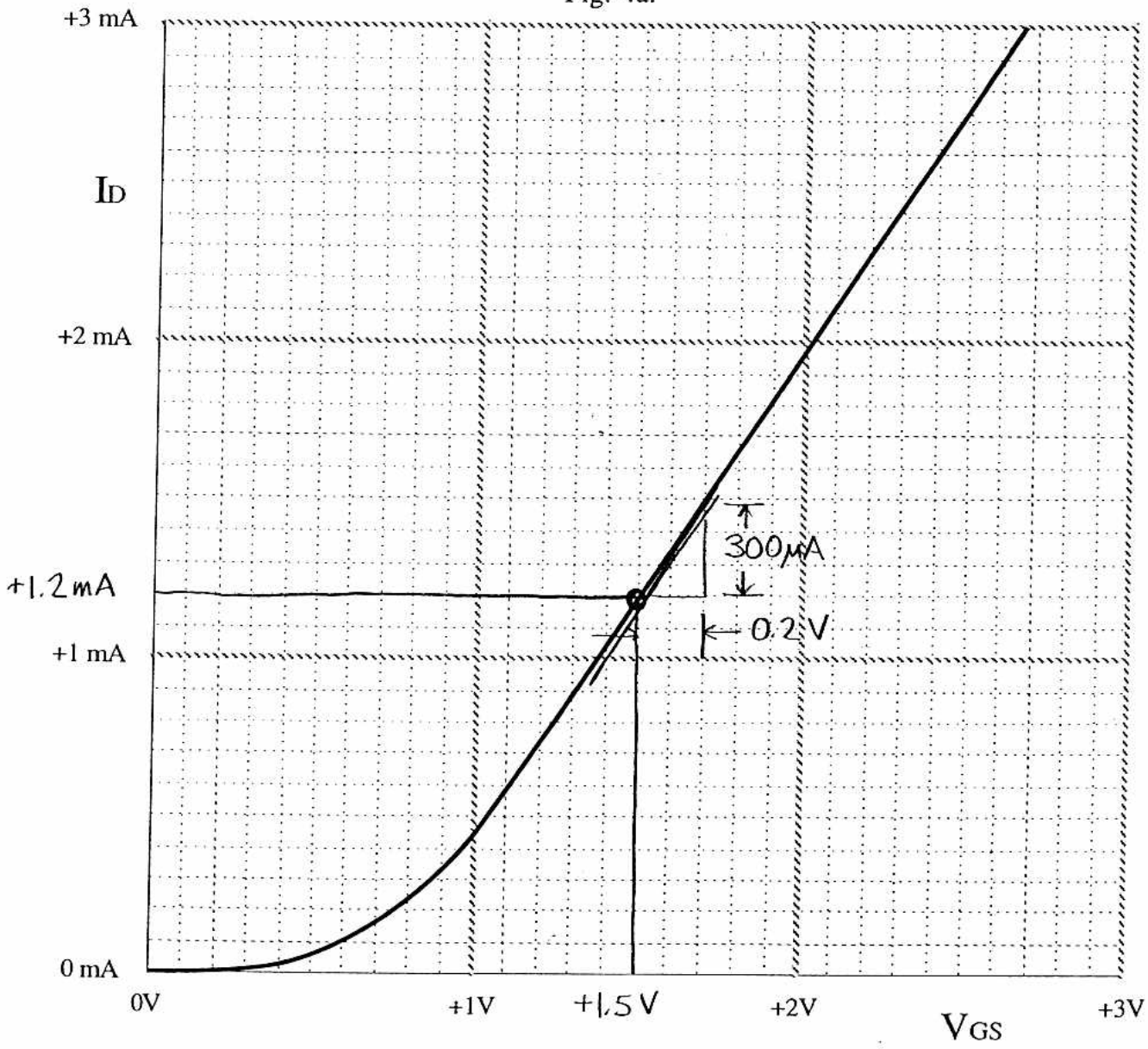
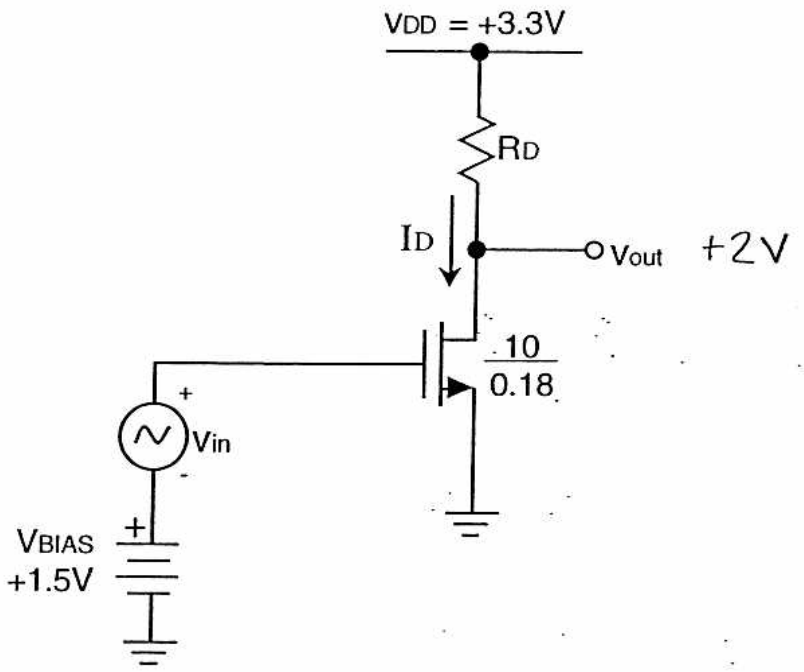


Fig. 4a.



It is desired to use this MOSFET in a common-source amplifier configuration shown below, in which the small-signal input rides on a +1.5V DC bias level.



a) Find the DC drain current I_D at this operating point. Indicate the operating point on the I_D-V_{GS} plot. [4]

$I_D =$ 1.2 mA FROM GRAPH

b) Determine the transconductance g_m at this operating point. [8]

$g_m =$ 1.5 mA/V $g_M = \frac{dI_D}{dV_{GS}}$ SLOPE FROM GRAPH $\frac{300\mu A}{0.2\,V}$

USE DEFINITION of g_M

c) Determine the value of R_D for an output DC bias level of +2.0V [4]

$R_D =$ 1.08 kΩ DROP ACROSS R_D $(3.3V - 2V) = (1.2\,mA)R_D \Rightarrow R_D = \frac{1.3V}{1.2mA}$ (I_D)

d) Determine the small signal gain $a_v = v_{out}/v_{in}$ of the circuit with your value of R_D. You may ignore channel length modulation. [4]

$a_v =$ −1.62 $-g_m R_D = \left(1.5\frac{mA}{V}\right)(1.08\,k\Omega) = -$